

AHA4702

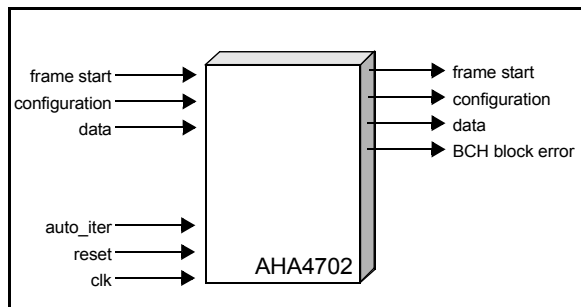
DVB-S2 Compliant LDPC/BCH Forward Error Correction (FEC) Decoder Core

INTRODUCTION

The AHA4702 FEC decoder core is fully compliant with section 5.3 of the Digital Video Broadcast S2 (DVB-S2) standard. It is capable of 85 Mbit/sec user data rate with a 2/3 rate LDPC Code and 25 iterations in an FPGA. The core supports all codes, frame sizes, and interleave schemes set forth in the DVB-S2 specification for broadcast, interactive, digital satellite news gathering, and professional services. The core allows code and modulation changes on a block-by-block basis to fully support both Adaptive Coding and Modulation (ACM) and Variable Coding and Modulation (VCM).

The AHA4702 FEC decoder core is comprised of a Low Density Parity Check (LDPC) inner code concatenated with a BCH outer code. It provides a wide range of code rates from 1/4 to 9/10 and interleave depths from 1 (no interleaving) to 5 bits/symbol. The ACM/VCM support allows configuration changes of the FEC core on a block-by-block basis while streaming without any data loss. In band signaling can control code and modulation changes for applications that use (ACM/VCM) schemes.

Figure 1: Block Diagram



FEATURES

ENCODER/DECODER:

- DVB-S2 compliant
- LDPC inner code with a BCH outer code
- 36 Msymb/s channel rate
- Supported codes: 1/4 through 9/10 code rates
- Supported block sizes: 16K and 64K block sizes
- Packet Error Rate performance to 10E-7
- Auto Iterations to optimize code performance
- Full ACM and VCM compliance

OTHERS

- Available as ASIC core upon request
- JTAG (available in ASIC version of the core)
- LLR demapper optionally available with FEC core.
- Available for both Altera and Xilinx FPGA platforms
- 155 Mbit/sec data rate in an ASIC

EVALUATION TOOLS

- For free evaluation software, please contact AHA.

DELIVERABLES

- Altera, Xilinx, or ASIC synthesized netlist.
- Complete Documentation
- Bit accurate C models

APPLICATIONS

- Broadcast TV, HDTV
- Satellite communications
- Microwave communications
- Cellular Backhaul

Table 1: DVB-S2 Codes and Performance

Code Rate	Spectral Efficiency (bits/symbol)	Ideal Es/No (dB) (QEF)	Eb/No (dB)
1/4	0.49	-2.4	0.6
1/3	0.66	-1.2	0.6
2/5	0.79	-0.3	0.7
1/2	0.99	1.0	1.0
3/5	1.19	2.2	1.4
2/3	1.32	3.1	1.9
3/4	1.49	4.0	2.2
4/5	1.59	4.7	2.7
5/6	1.65	5.2	3.0
8/9	1.77	6.2	3.7
9/10	1.79	6.4	3.8

In Table 1, configuration is 64K block size, QPSK modulation, and Quasi Error Free (QEF) on an AWGN Channel. The 16K codes perform about 0.2 to 0.3 dB worse. In addition to QPSK performance this design meets the performance data published in the DVB-S2 standard document for all of the other modulation schemes.

ORDERING INFORMATION

Part Number	Description
AHA4702	DVB-S2 LDPC Decoder Core

ABOUT AHA

Comtech AHA Corporation (AHA) develops and markets superior integrated circuits, boards, and intellectual property core technology for communications systems architects worldwide. AHA has been setting the standard in Forward Error Correction and Lossless Data Compression technology for many years and provides flexible, cost-effective solutions for today's growing bandwidth and reliability challenges. Comtech AHA Corporation is a wholly owned subsidiary of Comtech Telecommunications Corp. (NASDAQ: CMTL). For more information, visit www.aha.com



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