

Preliminary

Notice: This is not final specification.
Some parametric limits are subject to change.

M5M5T5636GP -25,22,20

18874368-BIT(524288-WORD BY 36-BIT) NETWORK SRAM

DESCRIPTION

The M5M5T5636GP is a family of 18M bit synchronous SRAMs organized as 524288-words by 36-bit. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Mitsubishi's SRAMs are fabricated with high performance, low power CMOS technology, providing greater reliability. M5M5T5636GP operates on 2.5V power/ 1.8V I/O supply or a single 2.5V power supply and are 2.5V CMOS compatible.

FEATURES

- Fully registered inputs and outputs for pipelined operation
- Fast clock speed: 250, 225 and 200 MHz
- Fast access time: 2.6, 2.8 and 3.2 ns
- Single 2.5V -5% and +5% power supply VDD
- Separate VDDQ for 2.5V or 1.8V I/O
- Individual byte write (BWA# - BWD#) controls may be tied LOW
- Single Read/Write control pin (W#)
- CKE# pin to enable clock and suspend operations
- Internally self-timed, registers outputs eliminate the need to control G#
- Snooze mode (ZZ) for power down
- Linear or Interleaved Burst Modes
- Three chip enables for simple depth expansion

Package

100pin TQFP

APPLICATION

High-end networking products that require high bandwidth, such as switches and routers.

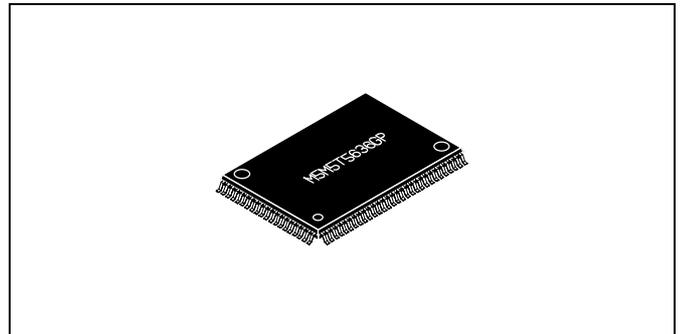
FUNCTION

Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition.

Synchronous signals include : all Addresses, all Data Inputs, all Chip Enables (E1#, E2, E3#), Address Advance/Load (ADV), Clock Enable (CKE#), Byte Write Enables (BWA#, BWb#, BWC#, BWD#) and Read/Write (W#). Write operations are controlled by the four Byte Write Enables (BWA# - BWD#) and Read/Write(W#) inputs. All writes are conducted with on-chip synchronous self-timed write circuitry.

Asynchronous inputs include Output Enable (G#), Clock (CLK) and Snooze Enable (ZZ). The HIGH input of ZZ pin puts the SRAM in the power-down state. The Linear Burst order (LBO#) is DC operated pin. LBO# pin will allow the choice of either an interleaved burst, or a linear burst.

All read, write and deselect cycles are initiated by the ADV LOW input. Subsequent burst address can be internally generated as controlled by the ADV HIGH input.



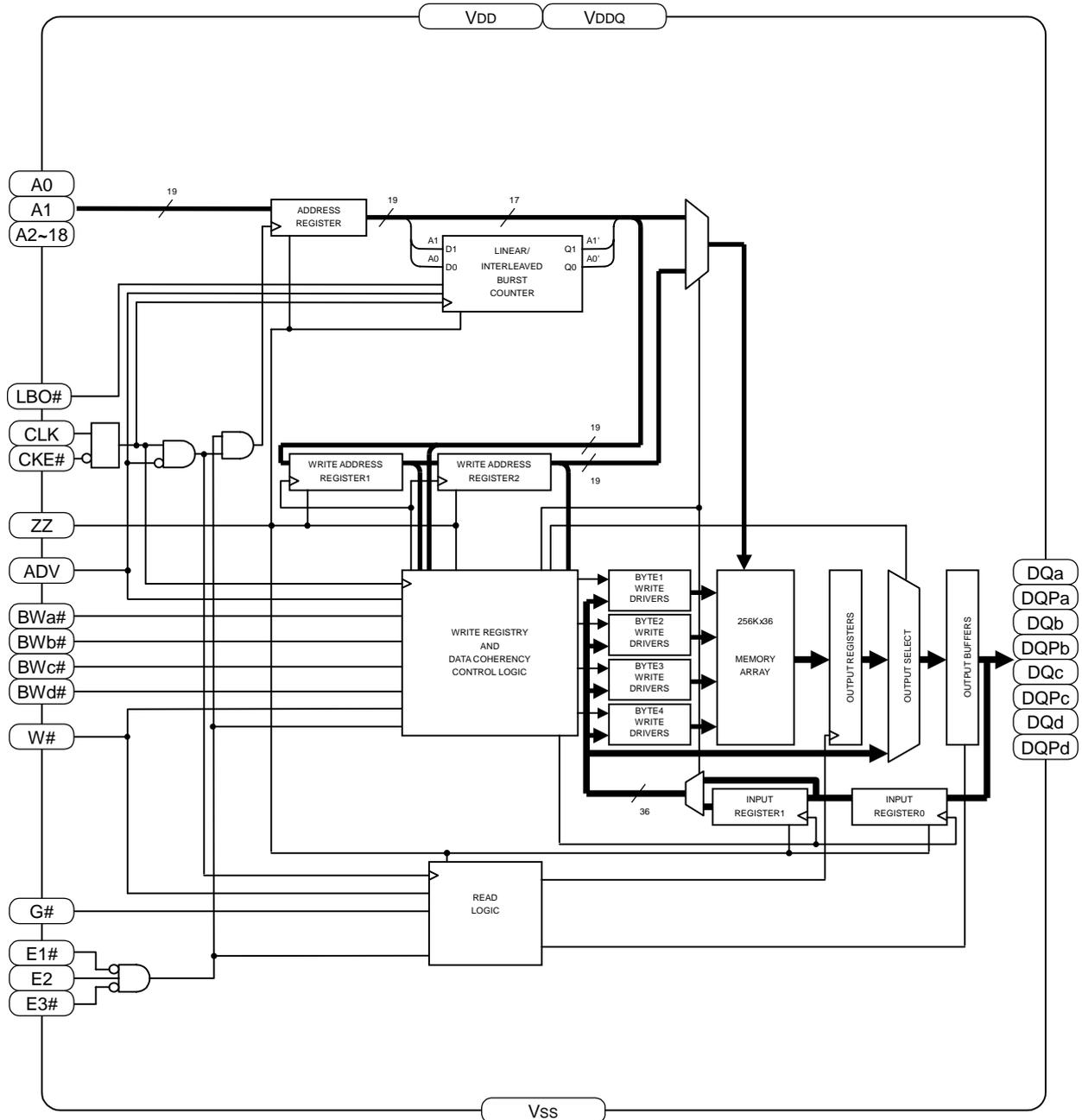
PART NAME TABLE

| Part Name | Access | Cycle | Active Current (max.) | Standby Current (max.) |
|------------------|--------|-------|-----------------------|------------------------|
| M5M5T5636GP - 25 | 2.6ns | 4.0ns | 560mA | 30mA |
| M5M5T5636GP - 22 | 2.8ns | 4.4ns | 500mA | 30mA |
| M5M5T5636GP - 20 | 3.2ns | 5.0ns | 440mA | 30mA |

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BLOCK DIAGRAM



Note2. The BLOCK DIAGRAM does not include the Boundary Scan logic.

Note3. The BLOCK DIAGRAM illustrates simplified device operation. See TRUTH TABLE, PIN FUNCTION and timing diagrams for detailed information.

PIN FUNCTION

| Pin | Name | Function |
|--|----------------------------------|---|
| A0~A18 | Synchronous Address Inputs | These inputs are registered and must meet the setup and hold times around the rising edge of CLK. A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired. |
| BWa#, BWb#, BWc#, BWd# | Synchronous Byte Write Enables | These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITES need to be asserted on the same cycle as the address. BWs are associated with addresses and apply to subsequent data. BWa# controls DQa, DQP a pins; BWb# controls DQb, DQP b pins; BWc# controls DQc, DQP c pins; BWd# controls DQd, DQP d pins. |
| CLK | Clock Input | This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| E1# | Synchronous Chip Enable | This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). |
| E2 | Synchronous Chip Enable | This active High input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). This input can be used for memory depth expansion. |
| E3# | Synchronous Chip Enable | This active Low input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). This input can be used for memory depth expansion. |
| G# | Output Enable | This active LOW asynchronous input enable the data I/O output drivers. |
| ADV | Synchronous Address Advance/Load | When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When HIGH, W# is ignored. A LOW on this pin permits a new address to be loaded at CLK rising edge. |
| CKE# | Synchronous Clock Enable | This active LOW input permits CLK to propagate throughout the device. When HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK. |
| ZZ | Snooze Enable | This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored. When this pin is LOW or NC, the SRAM normally operates. |
| W# | Synchronous Read/Write | This active input determines the cycle type when ADV is LOW. This is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on the pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus width WRITEs occur if all byte write enables are LOW. |
| DQa,DQP a,DQb,DQP b,DQc,DQP c,DQd,DQP d | Synchronous Data I/O | Byte "a" is DQa , DQP a pins; Byte "b" is DQb, DQP b pins; Byte "c" is DQc, DQP c pins; Byte "d" is DQd,DQP d pins. Input data must meet setup and hold times around CLK rising edge. |
| LBO# | Burst Mode Control | This DC operated pin allows the choice of either an interleaved burst or a linear burst. If this pin is HIGH or NC, an interleaved burst occurs. When this pin is LOW, a linear burst occurs, and input leak current to this pin. |
| VDD | VDD | Core Power Supply |
| VSS | VSS | Core Ground |
| VDDQ | VDDQ | I/O buffer Power supply |
| VSSQ | VSSQ | I/O buffer Ground |
| MCH | Must Connect High | These pins should be connected to HIGH |
| NC | No Connect | These pins are not internally connected and may be connected to ground. |

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DC OPERATED TRUTH TABLE

| Name | Input Status | Operation |
|------|--------------|----------------------------|
| LBO# | HIGH or NC | Interleaved Burst Sequence |
| | LOW | Linear Burst Sequence |

Note4. LBO# is DC operated pin.

Note5. NC means No Connection.

Note6. See BURST SEQUENCE TABLE about interleaved and Linear Burst Sequence.

BURST SEQUENCE TABLE

Interleaved Burst Sequence (when LBO# = HIGH or NC)

| Operation | A18~A2 | A1,A0 | | | |
|--------------------------------------|----------------|-------|------|------|------|
| First access, latch external address | A18~A2 | 0, 0 | 0, 1 | 1, 0 | 1, 1 |
| Second access(first burst address) | latched A18~A2 | 0, 1 | 0, 0 | 1, 1 | 1, 0 |
| Third access(second burst address) | latched A18~A2 | 1, 0 | 1, 1 | 0, 0 | 0, 1 |
| Fourth access(third burst address) | latched A18~A2 | 1, 1 | 1, 0 | 0, 1 | 0, 0 |

Linear Burst Sequence (when LBO# = LOW)

| Operation | A18~A2 | A1,A0 | | | |
|--------------------------------------|----------------|-------|------|------|------|
| First access, latch external address | A18~A2 | 0, 0 | 0, 1 | 1, 0 | 1, 1 |
| Second access(first burst address) | latched A18~A2 | 0, 1 | 1, 0 | 1, 1 | 0, 0 |
| Third access(second burst address) | latched A18~A2 | 1, 0 | 1, 1 | 0, 0 | 0, 1 |
| Fourth access(third burst address) | latched A18~A2 | 1, 1 | 0, 0 | 0, 1 | 1, 0 |

Note7. The burst sequence wraps around to its initial state upon completion.

TRUTH TABLE

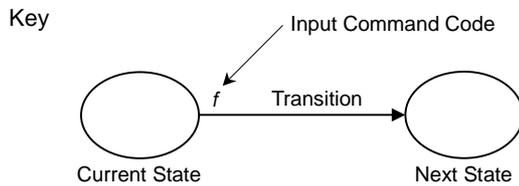
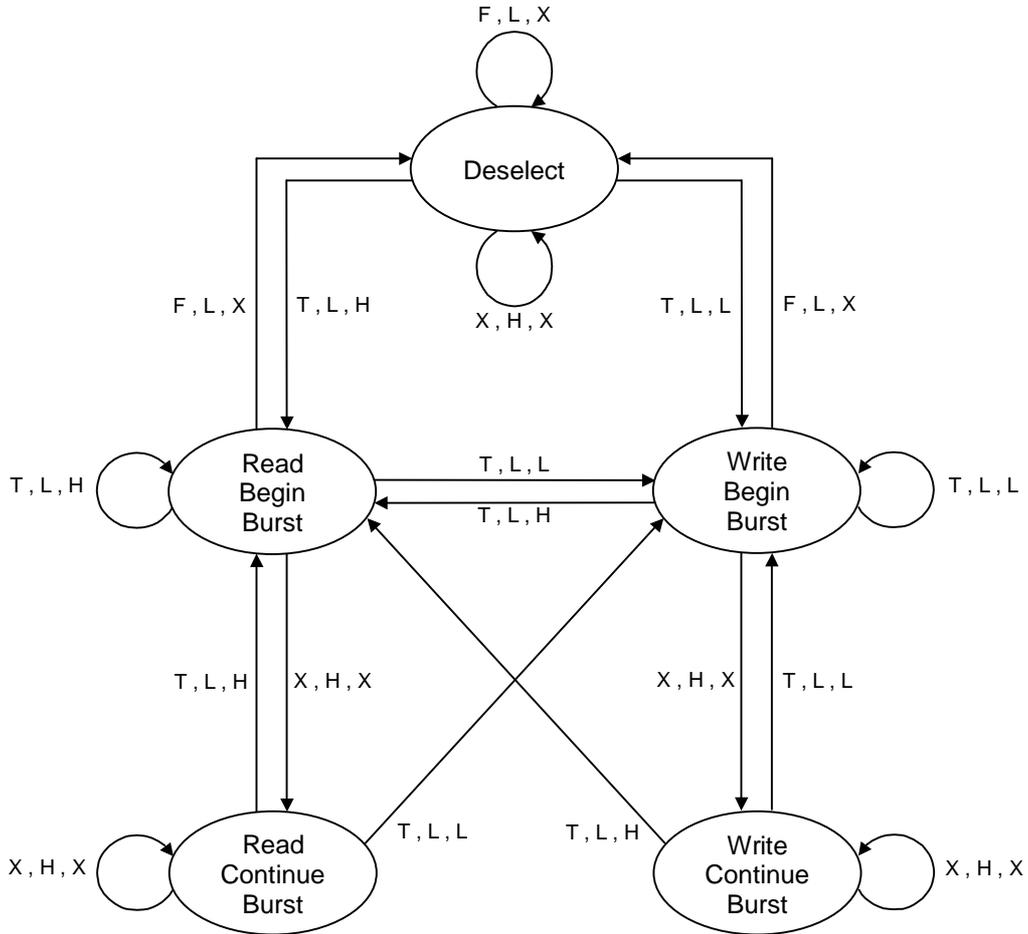
| E1# | E2 | E3# | ZZ | ADV | W# | BWx# | G# | CKE# | CLK | DQ | Address used | Operation |
|-----|----|-----|----|-----|----|------|----|------|------|--------|--------------|------------------------------|
| H | X | X | L | L | X | X | X | L | L->H | High-Z | None | Deselect Cycle |
| X | L | X | L | L | X | X | X | L | L->H | High-Z | None | Deselect Cycle |
| X | X | H | L | L | X | X | X | L | L->H | High-Z | None | Deselect Cycle |
| X | X | X | L | H | X | X | X | L | L->H | High-Z | None | Continue Deselect Cycle |
| L | H | L | L | L | H | X | L | L | L->H | Q | External | Read Cycle, Begin Burst |
| X | X | X | L | H | X | X | L | L | L->H | Q | Next | Read Cycle, Continue Burst |
| L | H | L | L | L | H | X | H | L | L->H | High-Z | External | NOP/Dummy Read, Begin Burst |
| X | X | X | L | H | X | X | H | L | L->H | High-Z | Next | Dummy Read, Continue Burst |
| L | H | L | L | L | L | L | X | L | L->H | D | External | Write Cycle, Begin Burst |
| X | X | X | L | H | X | L | X | L | L->H | D | Next | Write Cycle, Continue Burst |
| L | H | L | L | L | L | H | X | L | L->H | High-Z | None | NOP/Write Abort, Begin Burst |
| X | X | X | L | H | X | H | X | L | L->H | High-Z | Next | Write Abort, Continue Burst |
| X | X | X | L | X | X | X | X | H | L->H | - | Current | Ignore Clock edge, Stall |
| X | X | X | H | X | X | X | X | X | X | High-Z | None | Snooze Mode |

Note8. "H" = input VIH; "L" = input VIL; "X" = input VIH or VIL.

Note9. BWx#=H means all Synchronous Byte Write Enables (BWA#,BWb#,BWc#,BWd#) are HIGH. BWx#=L means one or more Synchronous Byte Write Enables are LOW.

Note10. All inputs except G# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

STATE DIAGRAM



Note11. The notation "x , x , x" controlling the state transitions above indicate the state of inputs E, ADV and W# respectively.
 Note12. If (E1# = L and E2 = H and E3# = L) then E="T" else E="F".
 Note13. "H" = input VIH; "L" = input VIL; "X" = input VIH or VIL; "T" = input "true"; "F" = input "false".

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WRITE TRUTH TABLE

| W# | BWa# | BWb# | BWc# | BWd# | Function |
|----|------|------|------|------|-----------------|
| H | X | X | X | X | Read |
| L | L | H | H | H | Write Byte a |
| L | H | L | H | H | Write Byte b |
| L | H | H | L | H | Write Byte c |
| L | H | H | H | L | Write Byte d |
| L | L | L | L | L | Write All Bytes |
| L | H | H | H | H | Write Abort/NOP |

Note14. "H" = input VIH; "L" = input VIL; "X" = input VIH or VIL.

Note15. All inputs except G# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------|---------------------------------|---------------------|-----------------|------|
| VDD | Power Supply Voltage | With respect to Vss | -1.0*~3.6 | V |
| VDDQ | I/O Buffer Power Supply Voltage | | -1.0*~3.6 | V |
| VI | Input Voltage | | -1.0~VDDQ+1.0** | V |
| VO | Output Voltage | | -1.0~VDDQ+1.0** | V |
| PD | Maximum Power Dissipation (VDD) | | 945 | mW |
| TOPR | Operating Temperature | | 0~70 | °C |
| TSTG(bias) | Storage Temperature(bias) | | -10~85 | °C |
| TSTG | Storage Temperature | | -65~150 | °C |

Note16.* This is -1.0V when pulse width≤2ns, and -0.5V in case of DC.

** This is -1.0V~VDDQ+1.0V when pulse width≤2ns, and -0.5V~VDDQ+0.5V in case of DC.

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DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, VDD=2.375~2.625V, unless otherwise noted)

| Symbol | Parameter | Condition | Limits | | Unit |
|--------|---|---|---------------------|-----------|------|
| | | | Min | Max | |
| VDD | Power Supply Voltage | | 2.375 | 2.625 | V |
| VDDQ | I/O Buffer Power Supply Voltage | VDDQ = 2.5V | 2.375 | 2.625 | V |
| | | VDDQ = 1.8V | 1.7 | 1.95 | |
| VIH | High-level Input Voltage | VDDQ = 2.375~2.625V | 1.7 | VDDQ+0.3* | V |
| | | VDDQ = 1.7~1.95V | 0.65*VDDQ | | |
| VIL | Low-level Input Voltage | VDDQ = 2.375~2.625V | -0.3* | 0.7 | V |
| | | VDDQ = 1.7~1.95V | | 0.35*VDDQ | |
| VOH | High-level Output Voltage | IOH = -2.0mA | VDDQ-0.4 | | V |
| VOL | Low-level Output Voltage | IOL = 2.0mA | | 0.4 | V |
| ILI | Input Leakage Current except ZZ and LBO# | VI = 0V ~ VDDQ | | 10 | μA |
| | Input Leakage Current of LBO# | VI = 0V ~ VDDQ | | 100 | |
| | Input Leakage Current of ZZ | VI = 0V ~ VDDQ | | 100 | |
| ILO | Off-state Output Current | VI (G#) ≥ VIH, VO = 0V ~ VDDQ | | 10 | μA |
| ICC1 | Power Supply Current : Operating | Device selected; Output Open VI ≤ VIL or VI ≥ VIH ZZ ≤ VIL | 4.0ns cycle(250MHz) | 560 | mA |
| | | | 4.4ns cycle(225MHz) | 500 | |
| | | | 5.0ns cycle(200MHz) | 440 | |
| ICC2 | Power Supply Current : Deselected | Device deselected VI ≤ VIL or VI ≥ VIH ZZ ≤ VIL | 4.0ns cycle(250MHz) | 260 | mA |
| | | | 4.4ns cycle(225MHz) | 220 | |
| | | | 5.0ns cycle(200MHz) | 180 | |
| ICC3 | CMOS Standby Current (CLK stopped standby mode) | Device deselected; Output Open VI ≤ VSS+0.2V or VI ≥ VDDQ-0.2V CLK frequency=0Hz, All inputs static | | 30 | mA |
| ICC4 | Snooze Mode Standby Current | Snooze mode ZZ ≥ VDDQ-0.2V, LBO# ≥ VDD-0.2V | | 30 | mA |
| ICC5 | Stall Current | Device selected; Output Open CKE# ≥ VIH VI ≤ VSS+0.2V or VI ≥ VDDQ-0.2V | 4.0ns cycle(250MHz) | 180 | mA |
| | | | 4.4ns cycle(225MHz) | 160 | |
| | | | 5.0ns cycle(200MHz) | 140 | |

Note17.*VILmin is -1.0V and VIHmax is VDDQ+1.0V in case of AC(Pulse width≤2ns).

Note18."Device Deselected" means device is in power-down mode as defined in the truth table.

CAPACITANCE

| Symbol | Parameter | Conditions | Limits | | | Unit |
|--------|--------------------------------|----------------------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| CI | Input Capacitance | VI=GND, VI=25mVrms, f=1MHz | | | 6 | pF |
| CO | Input / Output(DQ) Capacitance | Vo=GND, Vo=25mVrms, f=1MHz | | | 8 | pF |

Note19.This parameter is sampled.

THERMAL RESISTANCE

4-Layer PC board mounted (70x70x1.6mmT)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|--------|-------------------------------------|---------------------|--------|-------|-----|------|
| | | | Min | Typ | Max | |
| θJA | Thermal Resistance Junction Ambient | Air velocity=0m/sec | | 28.18 | | °C/W |
| | | Air velocity=2m/sec | | 20.33 | | °C/W |
| θJC | Thermal Resistance Junction to Case | | | 6.64 | | °C/W |

Note20.This parameter is sampled.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, VDD=2.375~2.625V, unless otherwise noted)

(1)MEASUREMENT CONDITION

- Input pulse levels VIH=VDDQ, VIL=0V
- Input rise and fall times faster than or equal to 1V/ns
- Input timing reference levels VIH=VIL=0.5*VDDQ
- Output reference levels VIH=VIL=0.5*VDDQ
- Output load Fig.1

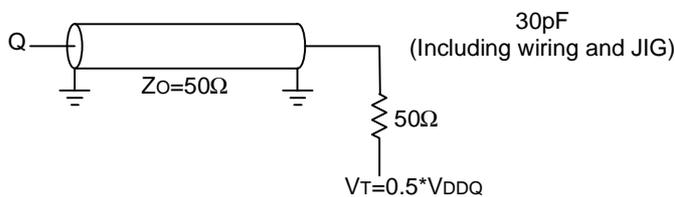


Fig.1 Output load

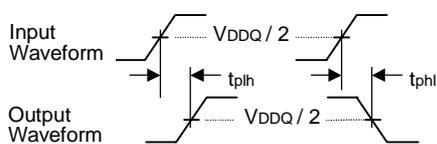


Fig.2 Tdly measurement

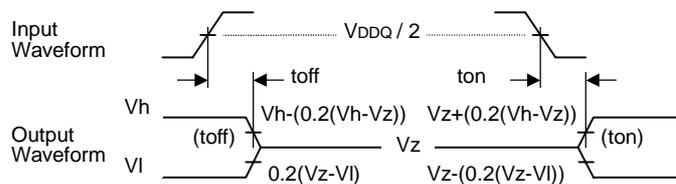


Fig.3 Tri-State measurement

Note21.Valid Delay Measurement is made from the VDDQ/2 on the input waveform to the VDDQ/2 on the output waveform.

Input waveform should have a slew rate of faster than or equal to 1V/ns.

Note22.Tri-state toff measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final Value VDDQ/2.

Note:the initial value is not VOL or VOH as specified in DC ELECTRICAL CHARACTERISTICS table.

Note23. Tri-state ton measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial Value VDDQ/2 to its final Value.

Note:the final value is not VOL or VOH as specified in DC ELECTRICAL CHARACTERISTICS table.

Note24.Clocks,Data,Address and control signals will be tested with a minimum input slew rate of faster than or equal to 1V/ns.

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(2)TIMING CHARACTERISTICS

| Symbol | Parameter | Limits | | | | | | Unit |
|--------------|---|--------|---------|--------|---------|--------|---------|------|
| | | 250MHz | | 225MHz | | 200MHz | | |
| | | -25 | | -22 | | -20 | | |
| | | Min | Max | Min | Max | Min | Max | |
| Clock | | | | | | | | |
| tKHKH | Clock cycle time | 4.0 | | 4.4 | | 5.0 | | ns |
| tKHKL | Clock HIGH time | 1.5 | | 1.6 | | 1.8 | | ns |
| tKLKH | Clock LOW time | 1.5 | | 1.6 | | 1.8 | | ns |
| Output times | | | | | | | | |
| tKHQV | Clock HIGH to output valid | | 2.6 | | 2.8 | | 3.2 | ns |
| tKHQX | Clock HIGH to output invalid | 1.5 | | 1.5 | | 1.5 | | ns |
| tKHQX1 | Clock HIGH to output in LOW-Z | 1.5 | | 1.5 | | 1.5 | | ns |
| tKHQZ | Clock HIGH to output in High-Z | 1.5 | 2.6 | 1.5 | 2.8 | 1.5 | 3.2 | ns |
| tGLQV | G# to output valid | | 2.6 | | 2.8 | | 3.2 | ns |
| tGLQX1 | G# to output in Low-Z | 0.0 | | 0.0 | | 0.0 | | ns |
| tGHQZ | G# to output in High-Z | | 2.6 | | 2.8 | | 3.2 | ns |
| Setup Times | | | | | | | | |
| tAVKH | Address valid to clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| tckeVKH | CKE# valid to clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| tadvVKH | ADV valid to clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| tWVKH | Write valid to clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| tBVKH | Byte write valid to clock HIGH (BWA#~BWD#) | 0.8 | | 1.0 | | 1.2 | | ns |
| tEVKH | Enable valid to clock HIGH (E1#,E2,E3#) | 0.8 | | 1.0 | | 1.2 | | ns |
| tDVKH | Data In valid clock HIGH | 0.8 | | 1.0 | | 1.2 | | ns |
| Hold Times | | | | | | | | |
| tKHAX | Clock HIGH to Address don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| tKHckeX | Clock HIGH to CKE# don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| tKHadvX | Clock HIGH to ADV don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| tKHwX | Clock HIGH to Write don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| tKHBX | Clock HIGH to Byte Write don't care (BWA#~BWB#) | 0.5 | | 0.5 | | 0.5 | | ns |
| tKHEx | Clock HIGH to Enable don't care (E1#,E2,E3#) | 0.5 | | 0.5 | | 0.5 | | ns |
| tKHdX | Clock HIGH to Data In don't care | 0.5 | | 0.5 | | 0.5 | | ns |
| ZZ | | | | | | | | |
| tZZS | ZZ standby | | 2*tKHKH | | 2*tKHKH | | 2*tKHKH | ns |
| tZZREC | ZZ recovery | | 2*tKHKH | | 2*tKHKH | | 2*tKHKH | ns |

Note25.All parameter except tZZS, tZZREC in this table are measured on condition that ZZ=LOW fix.

Note26.Test conditions is specified with the output loading shown in Fig.1 unless otherwise noted.

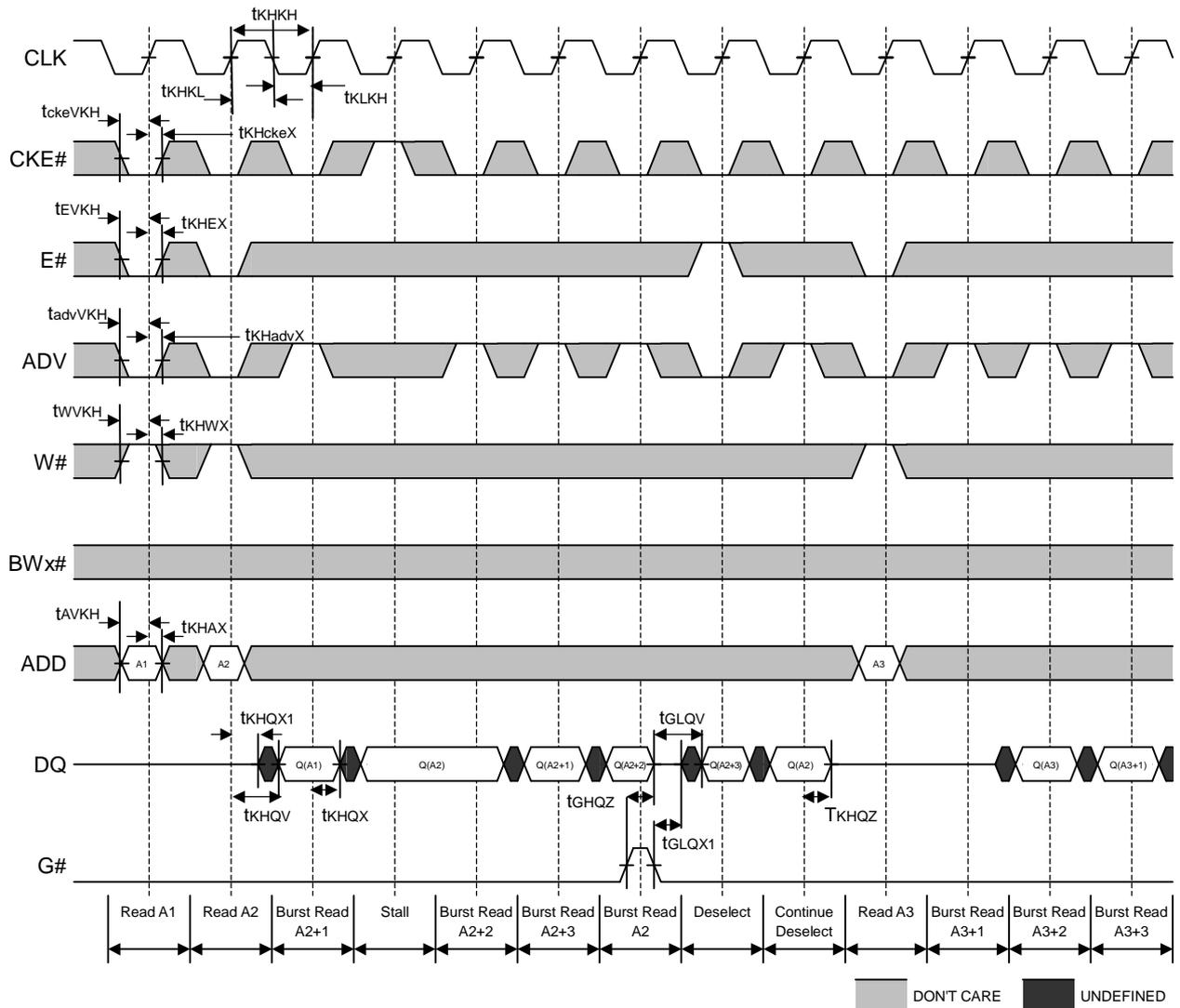
Note27. tKHQX1, tKHQZ, tGLQX1, tGHQZ are sampled.

Note28.LBO# is static and must not change during normal operation.

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(3)READ TIMING

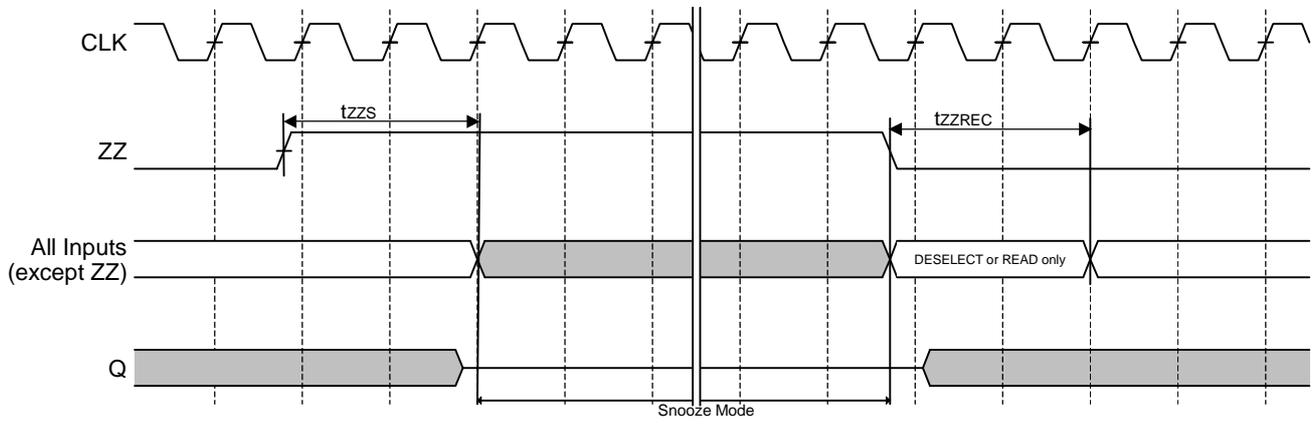


Note29. Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.

Note30. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.

Note31. ZZ is fixed LOW.

(6)SNOOZE MODE TIMING

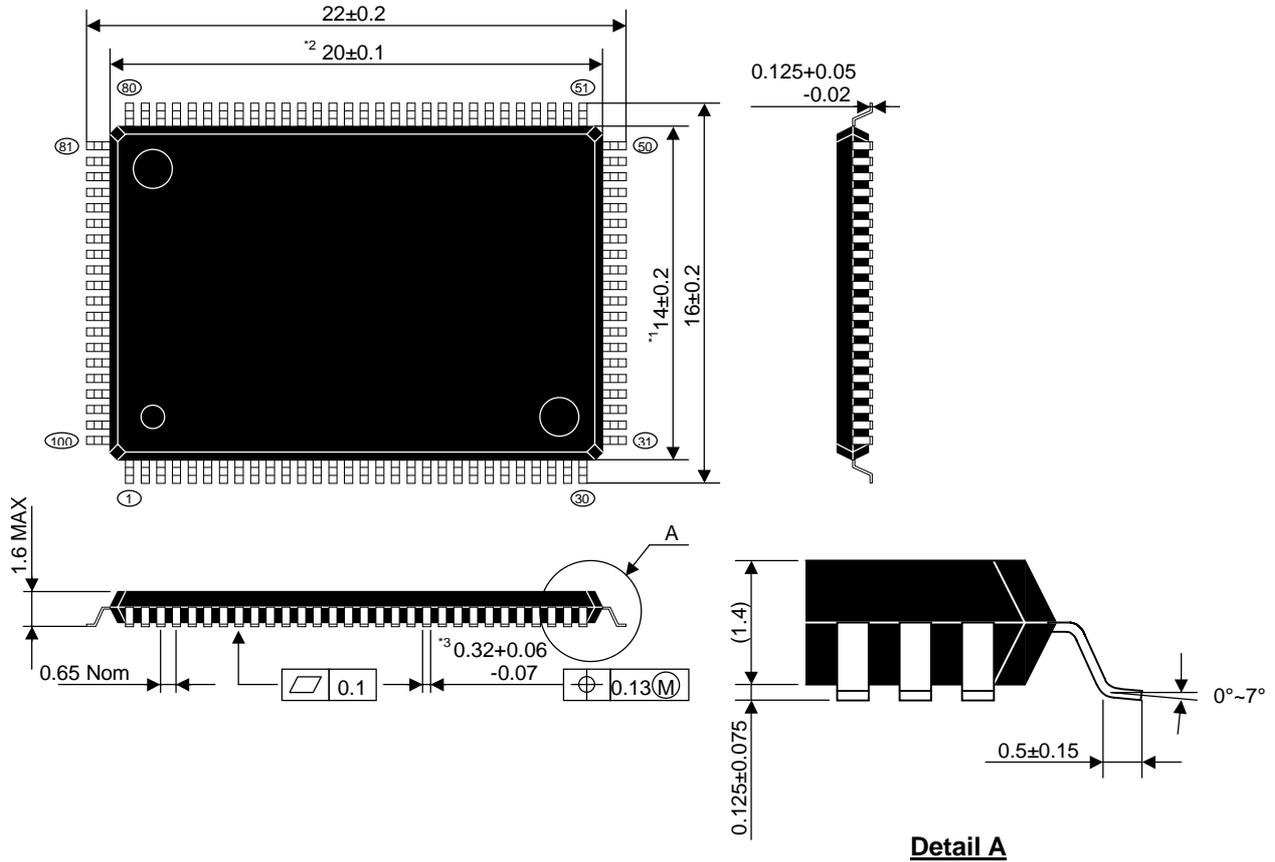


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PACKAGE OUTLINE

Plastic 100pin 14x20 mm body



Note38. Dimensions *1 and *2 don't include mold flash.
 Note39 Dimension *3 doesn't include trim off set.
 Note40. All dimensions in millimeters.

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REVISION HISTORY

| Rev. No. | History | Date | |
|----------|--|------------------|----------------------|
| 0.0 | First revision | June 4, 2001 | Advanced Information |
| 0.1 | Fixed WRITE TRUTH TABLE | July 16, 2001 | Advanced Information |
| 0.2 | Fixed Note8,13 and 14 | March 28, 2002 | Advanced Information |
| 0.3 | Add -13(133MHz) Fixed THERMAL RESISTANCE Preliminary | July 5, 2002 | Preliminary |
| 0.4 | DC ELECTRICAL CHARACTERISTICS Changed VIH limit from 0.65VDDQ to 1.7 at 2.5V VDDQ Changed VIL limit from 0.35VDDQ to 0.7 at 2.5V VDDQ Changed ICC1 limit from 380mA to 500mA at 225MHz(-22) Changed ICC1 limit from 360mA to 440mA at 200MHz(-20) Changed ICC2 limit from 110mA to 220mA at 225MHz(-22) Changed ICC2 limit from 100mA to 180mA at 200MHz(-20) Changed ICC5 limit from 60mA to 160mA at 225MHz(-22) Changed ICC5 limit from 50mA to 140mA at 200MHz(-20) AC ELECTRICAL CHARACTERISTICS Changed tKHQX limit from 0.6ns to 1.5ns at 225MHz(-22) Changed tKHQX limit from 0.7ns to 1.5ns at 200MHz(-20) Changed tKHQX1 limit from 0.6ns to 1.5ns at 225MHz(-22) Changed tKHQX1 limit from 0.7ns to 1.5ns at 200MHz(-20) Changed tKHQZ limit from 0.6ns to 1.5ns at 225MHz(-22) Changed tKHQZ limit from 0.7ns to 1.5ns at 200MHz(-20) | August 7, 2002 | Preliminary |
| 0.5 | DC ELECTRICAL CHARACTERISTICS Changed ILI limit from 10uA to 100uA (Input Leakage Current of ZZ and LBO#) Changed Icc3 and Icc4 limit from 20mA to 30mA (Standby Current) | January 14, 2003 | Preliminary |
| 0.6 | Added -25(250MHz) | January 31, 2003 | Preliminary |

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