

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

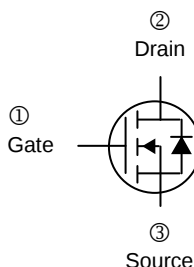
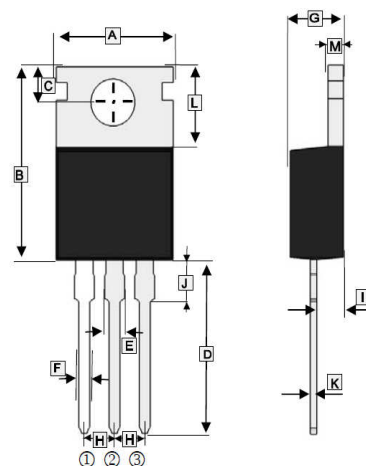
The SSE08N60SL is an N-channel enhancement mode power MOS field effect transistor which is produced. The improved planar strip cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 8A, 600V, $R_{DS(ON)(TYP.)}=0.96\Omega@V_{GS}=10V$
- Low Gate Charge
- Low C_{rss}
- Fast Switching
- Improved dv/dt Capability

TO-220P



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	9.3	10.6	H	2.54 BCS.	
B	14.2	16.5	I	1.8	2.9
C	2.7 BCS.		J	2.6	3.95
D	12.6	14.7	K	0.3	0.7
E	1.0	1.8	L	5.8	7.0
F	0.4	1.0	M	1.0	1.45
G	3.6	4.8			

ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	8	A
		5	A
Pulsed Drain Current	I_{DM}	32	A
Total Power Dissipation	P_D	147	W
		1.18	$^\circ\text{C} / \text{W}$
Single Pulse Avalanche Energy ¹	E_{AS}	450	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	0.85	$^\circ\text{C} / \text{W}$

Notes:

1. $L=30\text{mH}$, $I_{AS}=5\text{A}$, $V_{DD}=110\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	600	-	-	V	$V_{GS}=0, I_D= 250\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	$V_{GS}= \pm 30V, V_{DS}=0V$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=600V, V_{GS}=0V$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	0.96	1.2	Ω	$V_{GS}=10V, I_D=4A$
Total Gate Charge ^{1.2}	Q_g	-	14.83	-	nC	$I_D=8A$ $V_{DS}=480V$ $V_{GS}=10V$
Gate-Source Charge ^{1.2}	Q_{gs}	-	5.9	-		
Gate-Drain Change ^{1.2}	Q_{gd}	-	4	-		
Turn-on Delay Time ^{1.2}	$T_{d(on)}$	-	29	-	nS	$V_{DD}=300V$ $I_D=8A$ $R_G=25\ \Omega$
Rise Time ^{1.2}	T_r	-	71.33	-		
Turn-off Delay Time ^{1.2}	$T_{d(off)}$	-	34.93	-		
Fall Time ^{1.2}	T_f	-	32.8	-		
Input Capacitance	C_{iss}	-	910	-	pF	$V_{GS}=0$ $V_{DS}=25V$ $f=1.0MHz$
Output Capacitance	C_{oss}	-	105	-		
Reverse Transfer Capacitance	C_{rss}	-	2.43	-		
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	-	-	1.4	V	$I_S=8A, V_{GS}=0$
Continuous Source Current	I_S	-	-	8	A	Integral Reverse P-N Junction Diode in the MOSFET
Pulsed Source Current	I_{SM}	-	-	32	A	
Reverse Recovery Time	T_{rr}	-	520.65	-	ns	$I_S=8A, V_{GS}=0,$ $di_f/dt=100A/\mu S$
Reverse Recovery Charge	Q_{rr}	-	3.72	-	μC	

Notes:

1. Pulse Test: Pulse width $\leq 300\mu\text{S}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature.

CHARACTERISTIC CURVES

Figure 1. On-Region Characteristics

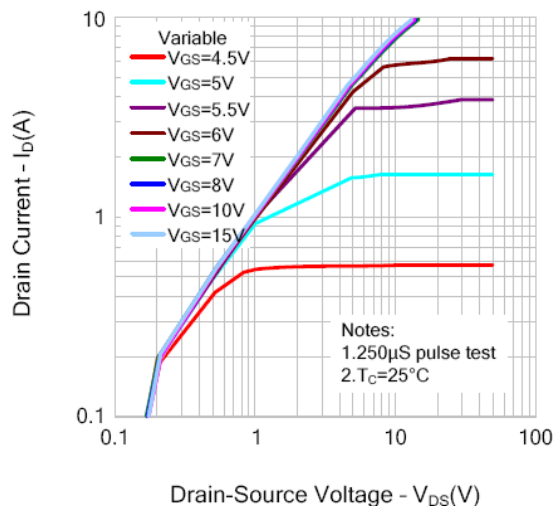


Figure 2. Transfer Characteristics

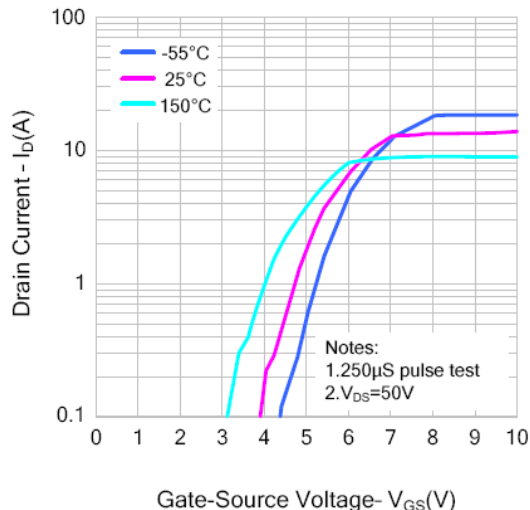


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

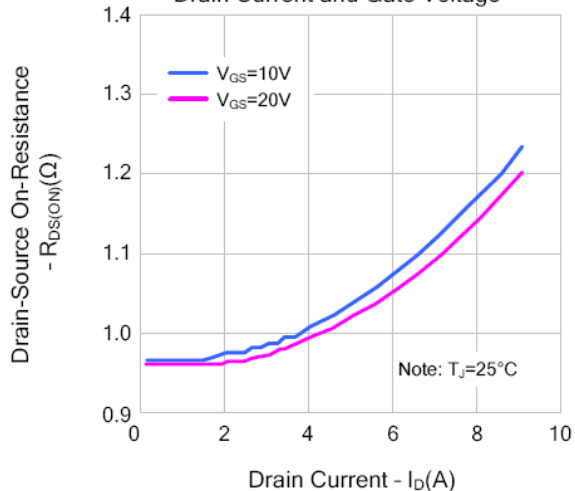


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

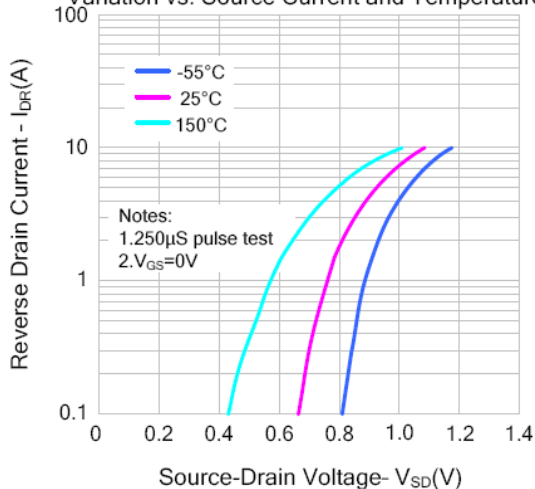


Figure 5. Capacitance Characteristics

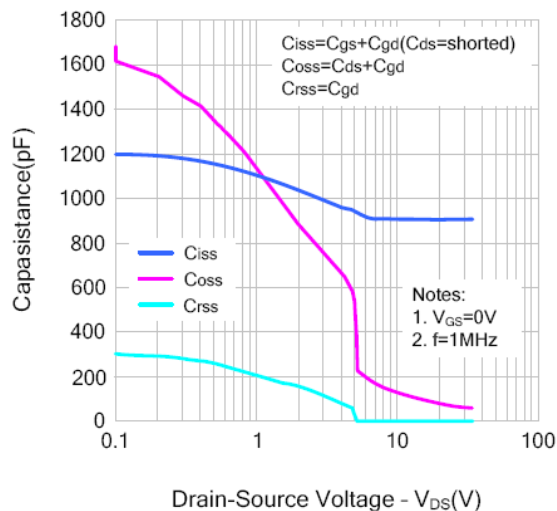
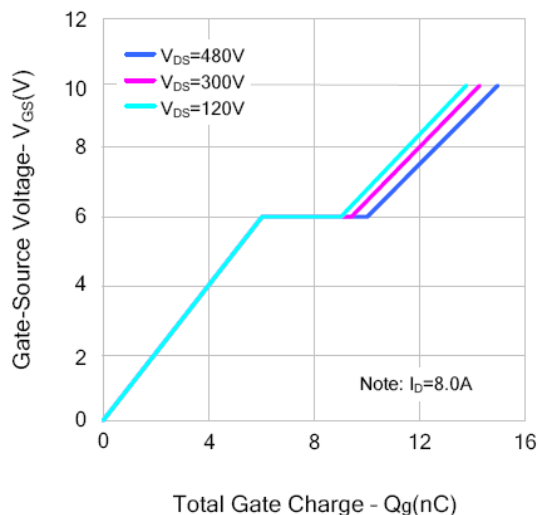


Figure 6. Gate Charge Characteristics



CHARACTERISTIC CURVES

Figure 7. Breakdown Voltage Variation vs. Temperature

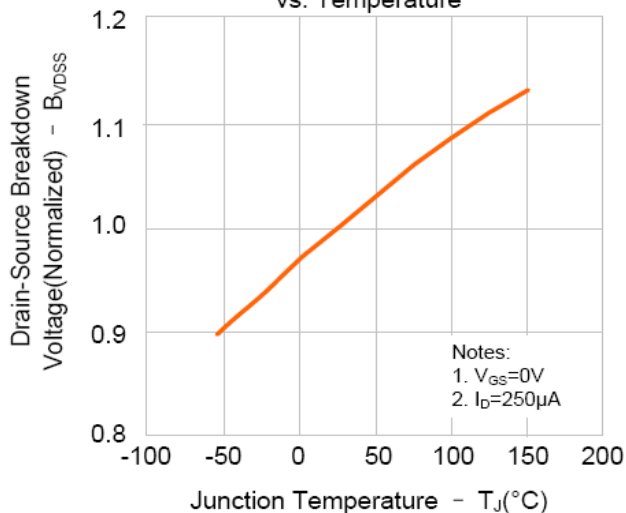


Figure 8. On-resistance Variation vs. Temperature

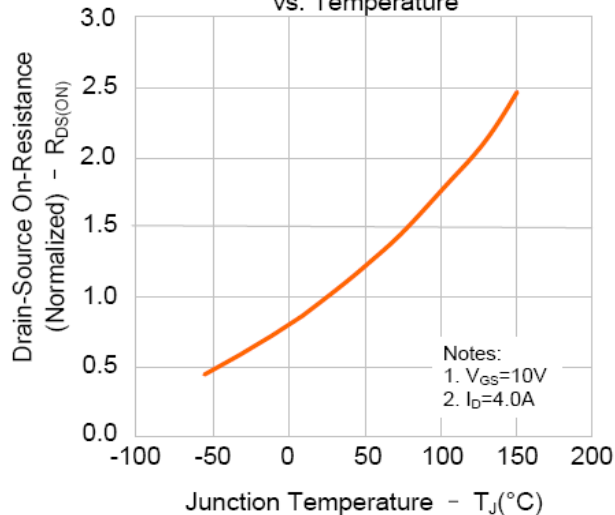


Figure 9-1. Max. Safe Operating Area

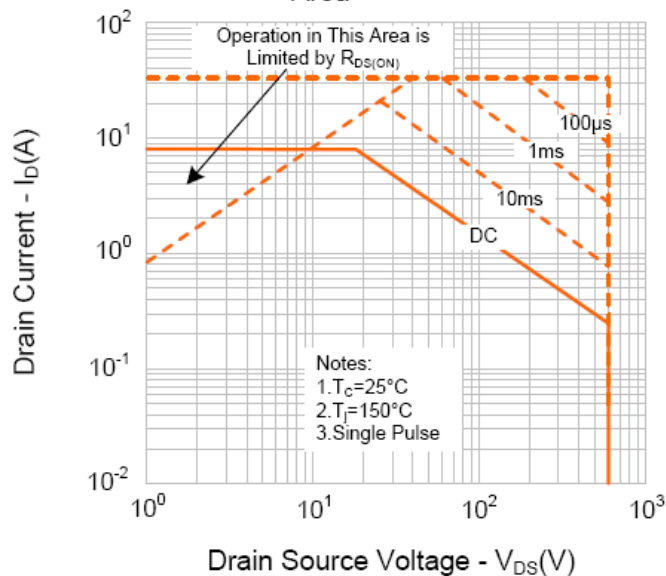
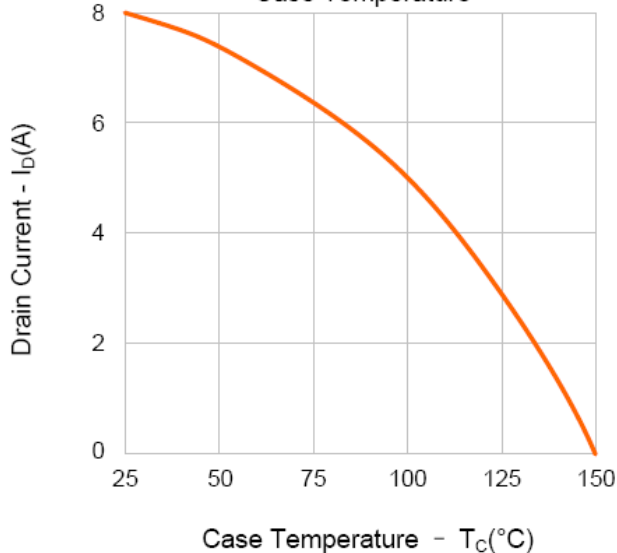
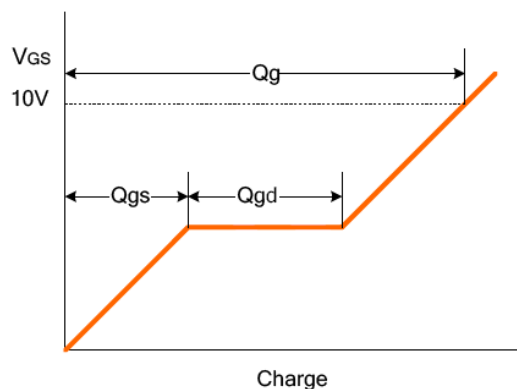
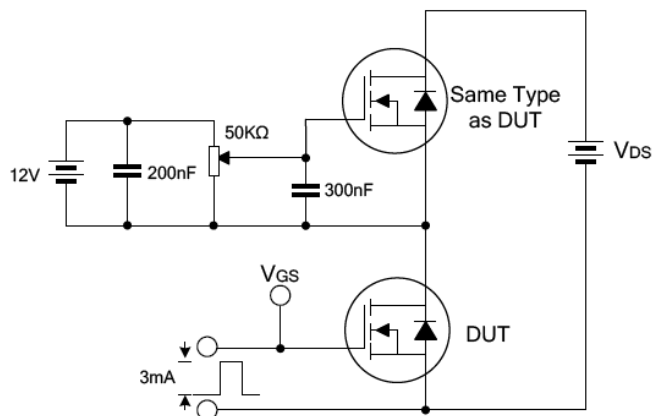


Figure 10. Maximum Drain Current vs. Case Temperature

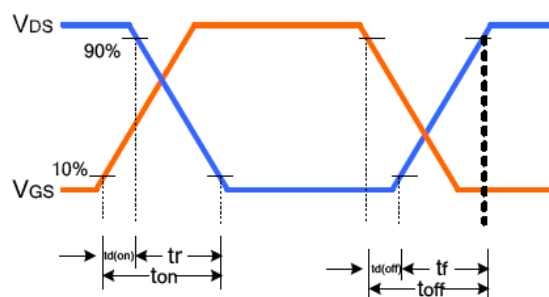
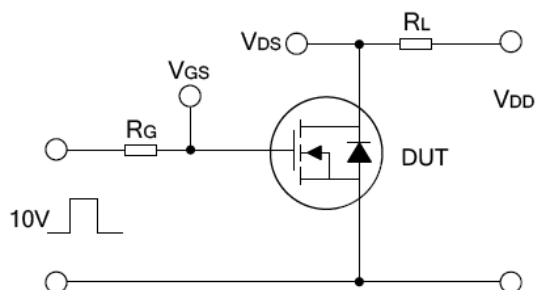


TYPICAL TEST CURVES

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

