Elektronische Bauelemente

SSG13P03

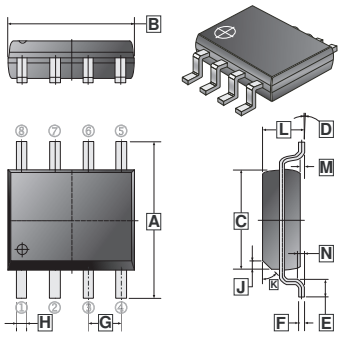
-13 A, -30 V, $R_{DS(ON)}$ 15 mΩ
P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSG13P03 uses advanced trench technology to provide excellent on-resistance, low gate charge and operation with gate voltages as low as 2.5V. The device is suitable for use as a load switch or in PWM applications. It may be used in a common drain arrangement to from a bidirectional blocking switch.

SOP-8

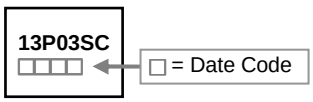


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

FEATURES

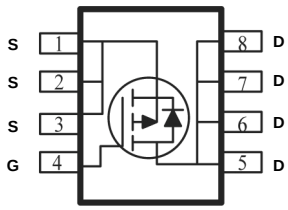
- Simple Drive Requirement
- Lower On-resistance
- Low Gate Charge

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13' inch



MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @ V_{GS}=10V [1]	T_A= 25℃	I_D	-13	A
	T_A=70℃		-8.2	
Pulsed Drain Current [2]		I_{DM}	-50	A
Single Pulse Avalanche Energy [3]		EAS	273	mJ
Avalanche Current		I_{AS}	-42	A
Total Power Dissipation [4]	T_A= 25℃	P_D	1.5	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient [1] (Max.)		$R_{\theta JA}$	85	℃ / W
Thermal Resistance Junction-Case [1] (Max.)		$R_{\theta JC}$	50	℃ / W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test condition
Static							
Drain-Source Breakdown Voltage		BV_{DSS}	-30	-	-	V	V_{GS}=0V, I_D= -250μA
Gate-Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D = -250μA
Forward Transfer Conductance		G_{fs}	-	32	-	S	V_{DS}= -5V, I_D= -8A
Gate-Body Leakage		I_{GSS}	-	-	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current	T_J =25°C	I_{DSS}	-	-	-1	μA	V_{DS}= -24V,V_{GS}=0
	T_J =55°C		-	-	-5		
Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	15	mΩ	V_{GS}= -10V, I_D = -8A
			-	-	20		V_{GS}= -4.5V, I_D = -6A
Total Gate Charge		Q_g	-	21.8	-	nC	I_D= -8A V_{DS}= -15V V_{GS}= -4.5V
Gate-Source Charge		Q_{gs}	-	7.9	-		
Gate-Drain (“Miller”) Charge		Q_{gd}	-	6.5	-		
Turn-On Delay Time [2]		$T_{d(on)}$	-	10	-	nS	V_{DS}= -15V I_D= -8A V_{GS}= -10V R_G= 3.3Ω
Rise Time		T_r	-	9.6	-		
Turn-Off Delay Time		$T_{d(off)}$	-	86	-		
Fall Time		T_f	-	9.6	-		
Input Capacitance		C_{iss}	-	2215	-	pF	V_{GS}=0V V_{DS}= -15V f=1.0MHz
Output Capacitance		C_{oss}	-	310	-		
Reverse Transfer Capacitance		C_{rss}	-	237	-		
Gate Resistance		R_G	-	9	18	Ω	f=1.0MHz
Avalanche Characteristics							
Single Pulse Avalanche Energy [5]		EAS	63	-	-	mJ	V_{DD}= -25V, L=0.1mH, I_{AS}= -21A
Source-Drain Diode							
Forward On Voltage [2]		V_{DS}	-	-	-1	V	I_S= -1A, V_{GS}=0V, T_J=25°C
Continuous Source Current [1.6]		I_S	-	-	-13	A	V_G= V_D=0V Force Current
Pulsed Source Current [2.6]		I_{SM}	-	-	-50	A	
Reverse Recovery Time		T_{RR}	-	16	-	nS	I_F=-8A, dI/dt=100A/μs, T_J=25°C
Reverse Recovery Charge		Q_{RR}	-	8	-	nC	

Notes:

1. surface mounted on a 1 inch2 FR-4 board with 2OZ copper. 125℃/W when mounted on Min. copper pad.
2. The data tested by pulsed , pulse width≦300us , duty cycle≦2%
3. The EAS data shows Max. rating . The test condition is V_{DD}= -25V,V_{GS}= -10V,L=0.1mH,I_{AS}= -50A
4. The power dissipation is limited by 150℃ junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

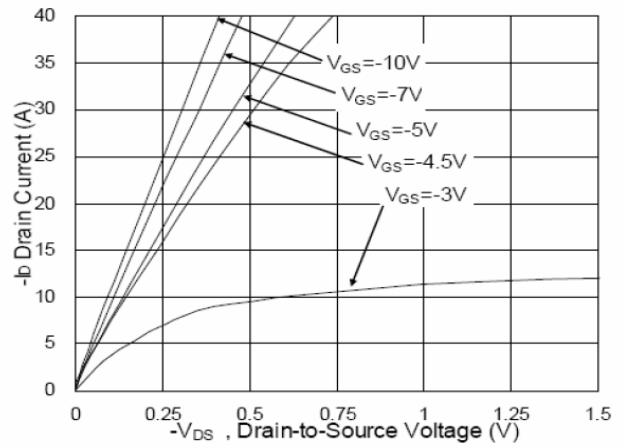


Fig.1 Typical Output Characteristics

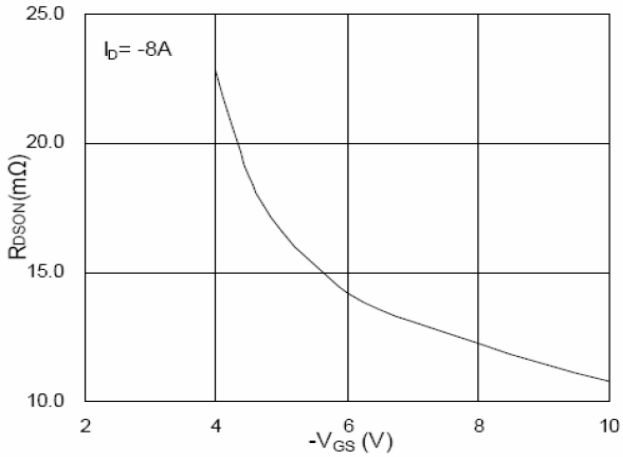


Fig.2 On-Resistance vs. G-S Voltage

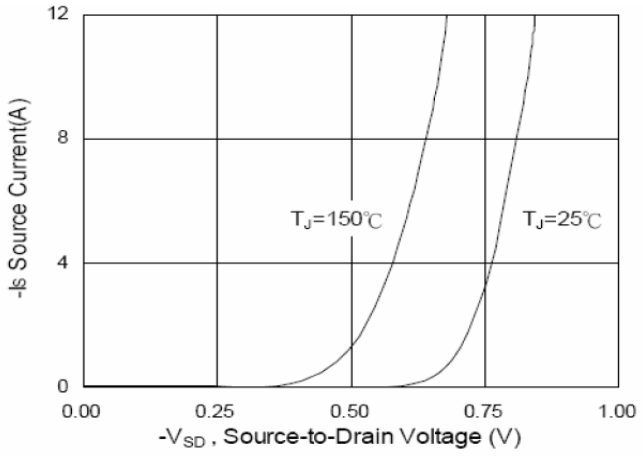


Fig.3 Forward Characteristics of Reverse

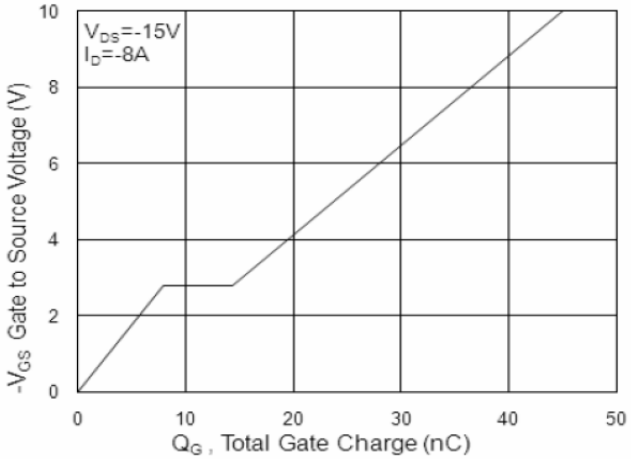


Fig.4 Gate-Charge Characteristics

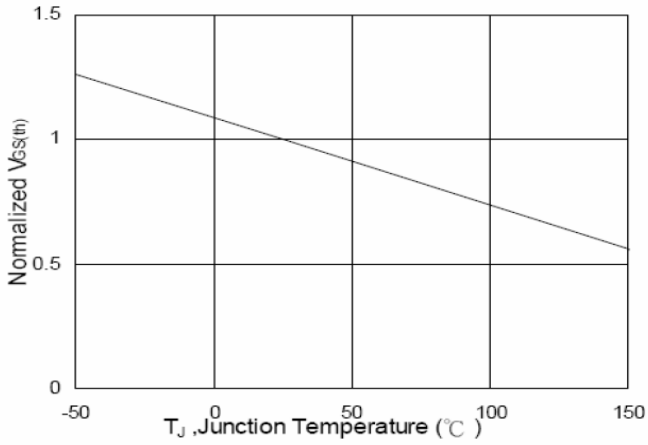


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

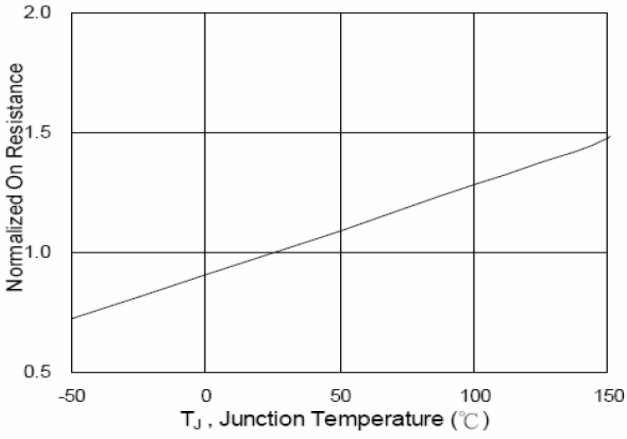


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVES

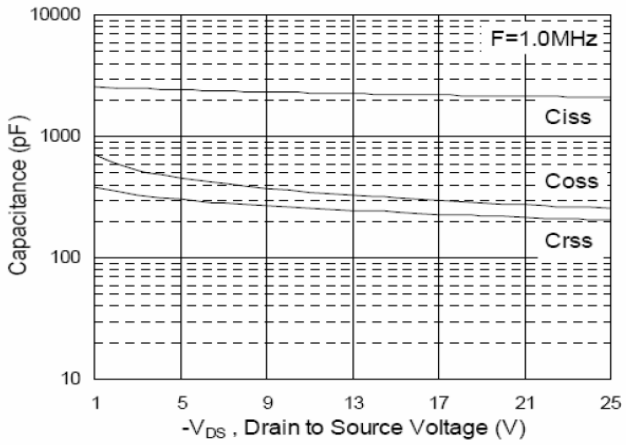


Fig.7 Capacitance

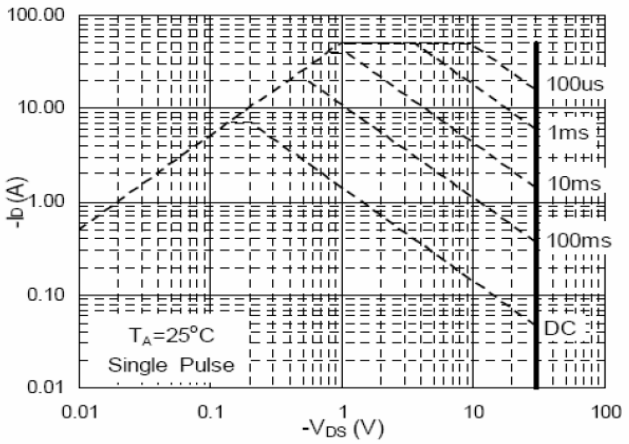


Fig.8 Safe Operating Area

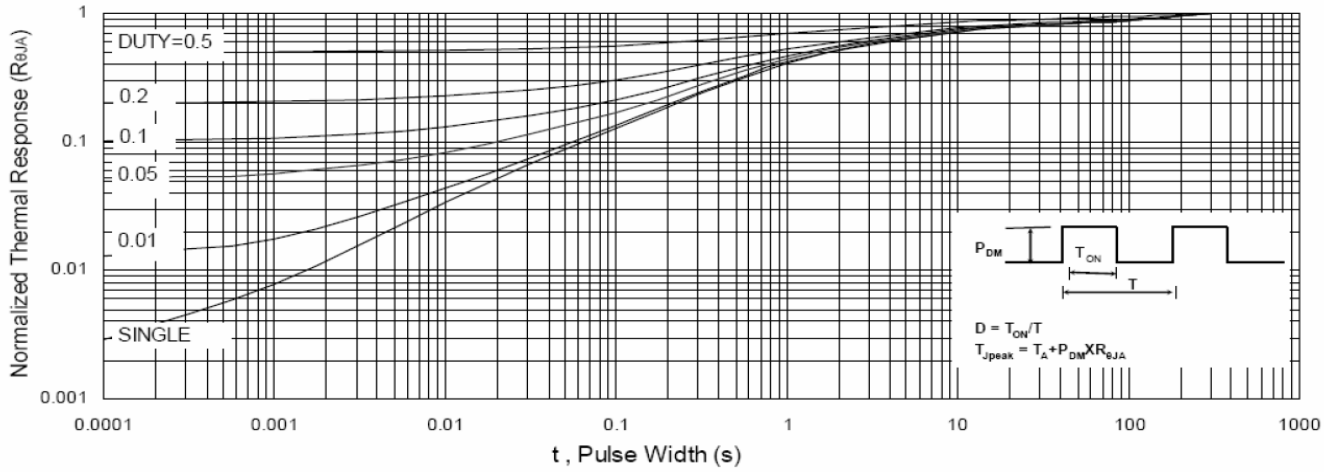


Fig.9 Normalized Maximum Transient Thermal Impedance

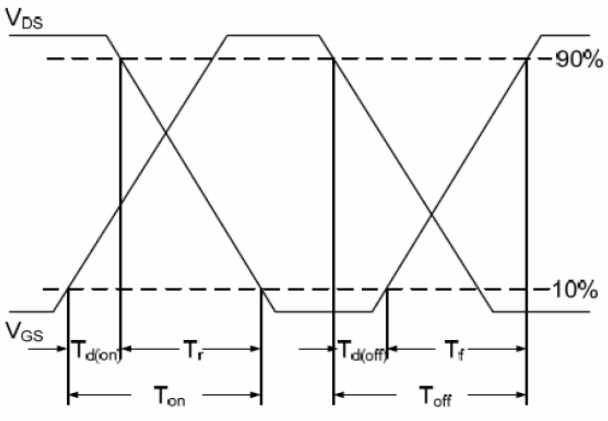


Fig.10 Switching Time Waveform

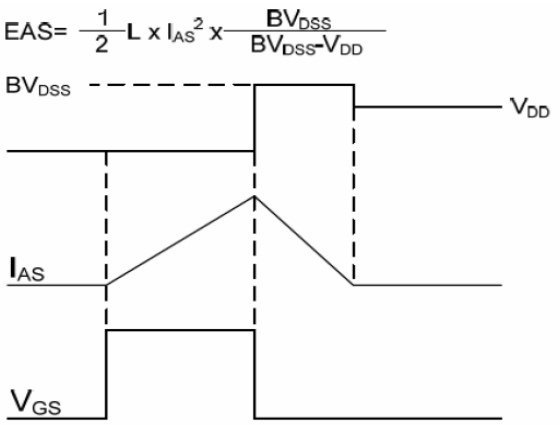


Fig.11 Unclamped Inductive Switching Wave