Elektronische Bauelemente

SSG2601

N & P-Ch Enhancement Mode Power MOSFET

N-Ch: 6.3 A, 20 V, $R_{DS(ON)}$ 25 mΩ

P-Ch: -5.3A, -20 V, $R_{DS(ON)}$ 75 mΩ

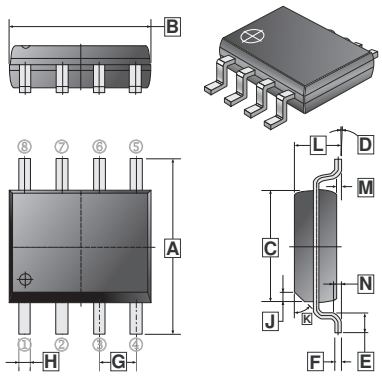
RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSG2601 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

SOP-8

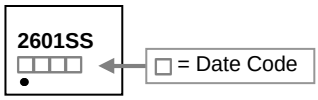


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

FEATURES

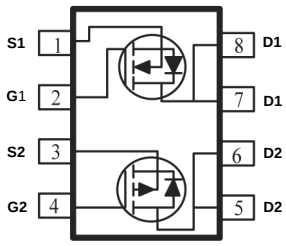
- Simple Drive Requirement
- Lower On-resistance
- Fast Switching Performance

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13 inch



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings		Unit
			N-Ch	P-Ch	
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current[1], V_{GS}@4.5V	T_A=25°C	I_D	6.3	-5.3	A
	T_A=70°C		4.9	-4	A
Pulsed Drain Current[2]		I_{DM}	25	-23	A
Total Power Dissipation[3]	T_A=25°C	P_D	1.5		W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		°C
Thermal Data					
Thermal Resistance Junction-ambient[1] Max.		$R_{\theta JA}$	85		°C / W
Thermal Resistance Junction-case[1] Max.		$R_{\theta JC}$	40		°C / W

N-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	20	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage		$V_{GS(th)}$	0.5	-	1	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transconductance		g_{fs}	-	25	-	S	V_{DS}=5V, I_D=6A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS} = ±12V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	uA	V_{DS}=16V, V_{GS}=0
	T_J=55°C		-	-	5		
Static Drain-Source On-Resistance[2]		$R_{DS(ON)}$	-	-	25	mΩ	V_{GS}=4.5V, I_D=5.3A
			-	-	34		V_{GS}=2.5V, I_D=5A
Total Gate Charge[2]		Q_g	-	9.5	-	nC	I_D=6A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge		Q_{gs}	-	1.33	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	2.5	-		
Turn-on Delay Time[2]		$T_{d(on)}$	-	4.6	-	nS	V_{DS}=10V V_{GS}=4.5V I_D=6A R_G=3.3Ω
Rise Time		T_r	-	32	-		
Turn-off Delay Time		$T_{d(off)}$	-	25.6	-		
Fall Time		T_f	-	8.4	-		
Input Capacitance		Ciss	-	635	-	pF	V_{GS}=0 V_{DS}=15V f=1.0MHz
Output Capacitance		Coss	-	70	-		
Reverse Transfer Capacitance		Crss	-	63	-		
Source-Drain Diode							
Forward On Voltage[2]		V_{SD}	-	-	1.2	V	I_S=1.2A, V_{GS}=0, T_j=25°C
Continuous Source Current [1,4]		I_S	-	-	6.3	A	V_D= V_G=0, Force Current
Pulsed Source Curren[2,4]		I_{SM}	-	-	25	A	

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 20Z copper. 135℃/ W when mounted on Min. copper pad.
2. The date tested by pulse width≦300us, duty cycle≦2%.
3. The power dissipation is limited by 150℃ juncti on temperature.
4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

P-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-20	-	-	V	V_{GS}=0, I_D= -250uA
Gate Threshold Voltage		$V_{GS(th)}$	-0.5	-	-1	V	V_{DS}=V_{GS}, I_D= -250uA
Forward Transconductance		g_{fs}	-	12	-	S	V_{DS}= -5V, I_D= -4A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±12V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	-1	uA	V_{DS}= -16V, V_{GS}=0
	T_J=55°C		-	-	-5		
Static Drain-Source On-Resistance[2]		$R_{DS(ON)}$	-	-	75	mΩ	V_{GS}= -4.5V, I_D= -4.2A
			-	-	105		V_{GS}= -2.5V, I_D= -3.8A
Total Gate Charge		Q_g	-	10	-	nC	I_D= -4A V_{DS}= -15V V_{GS}= -4.5V
Gate-Source Charge		Q_{gs}	-	1.93	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	3.18	-		
Turn-on Delay Time[2]		$T_{d(on)}$	-	5.6	-	nS	V_{DS}= -10V V_{GS}= -4.5V I_D= -4A R_G=3.3Ω
Rise Time		T_r	-	47.4	-		
Turn-off Delay Time		$T_{d(off)}$	-	31.6	-		
Fall Time		T_f	-	17.2	-		
Input Capacitance		Ciss	-	857	-	pF	V_{GS}=0 V_{DS}= -15V f=1.0MHz
Output Capacitance		Coss	-	114	-		
Reverse Transfer Capacitance		Crss	-	108	-		
Source-Drain Diode							
Forward On Voltage[2]		V_{SD}	-	-	-1.2	V	I_S= -1.2A, V_{GS}=0V, T_j=25°C
Continuous Source Current [1,4]		I_S	-	-	-5.3	A	V_D= V_G=0, Force Current
Pulsed Source Curren[2,4]		I_{SM}	-	-	-23	A	

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 20Z copper. 135℃/ W when mounted on Min. copper pad.
2. The date tested by pulse width≦300us, duty cycle≦2%.
3. The power dissipation is limited by 150℃ juncti on temperature.
4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVE (N-Ch)

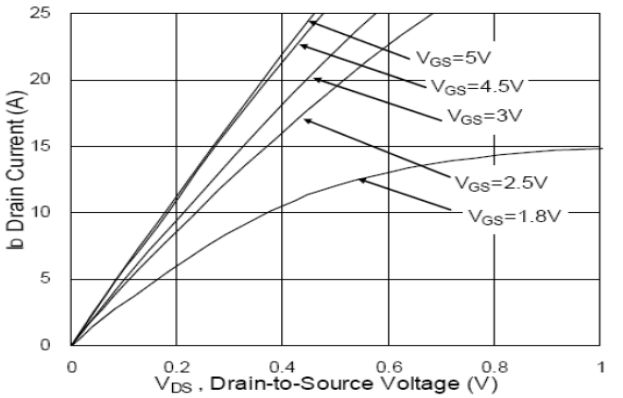


Fig.1 Typical Output Characteristics

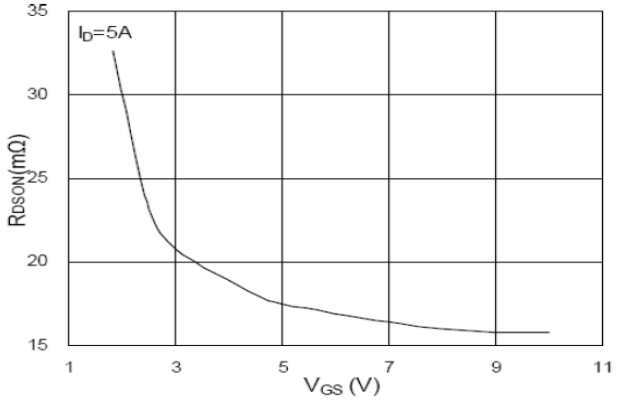


Fig.2 On-Resistance vs. Gate-Source

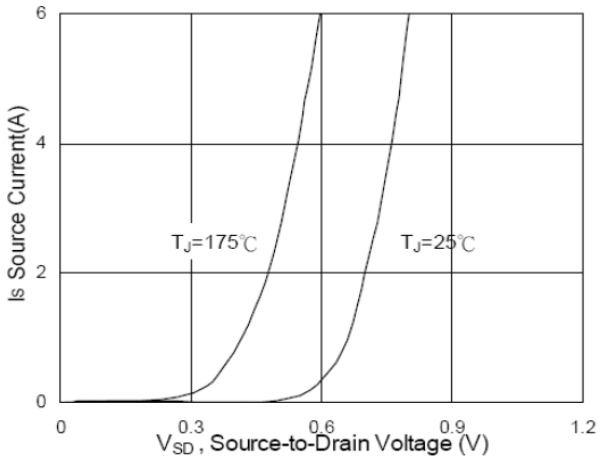


Fig.3 Forward Characteristics of Reverse

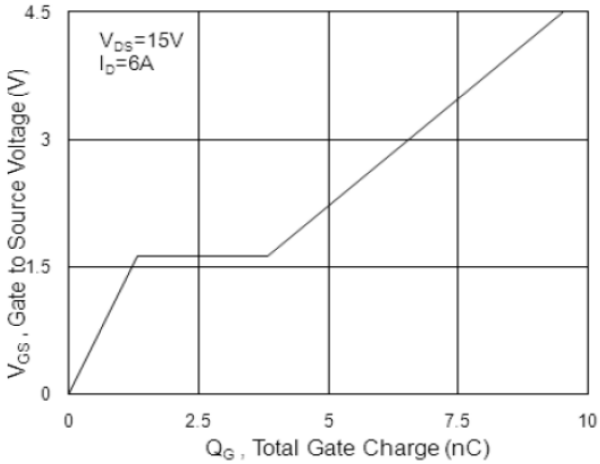


Fig.4 Gate-Charge Characteristics

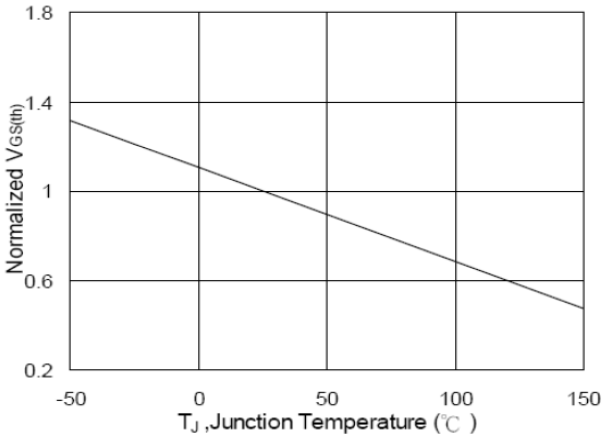


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

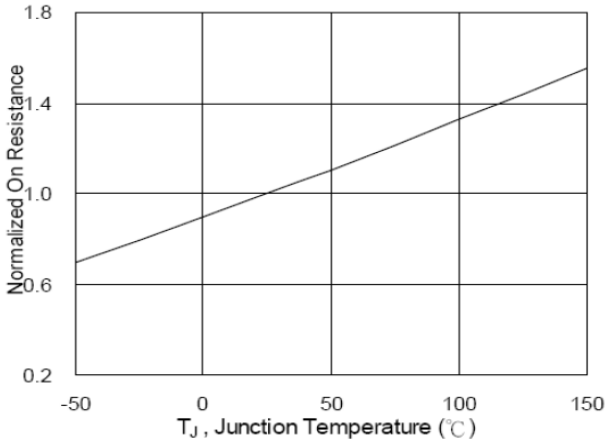


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVE (N-Ch)

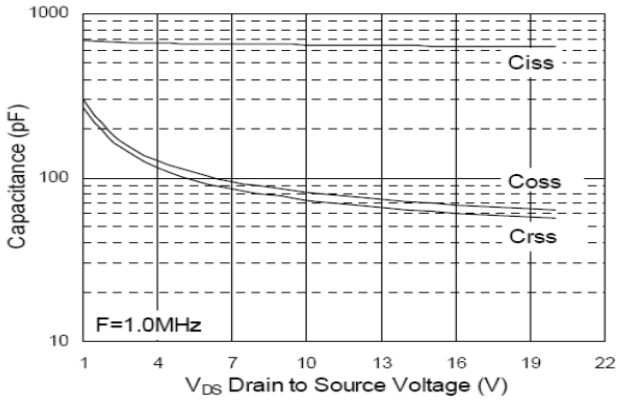


Fig.7 Capacitance

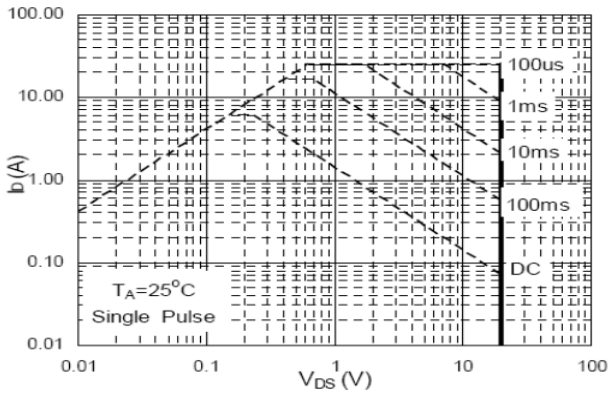


Fig.8 Safe Operating Area

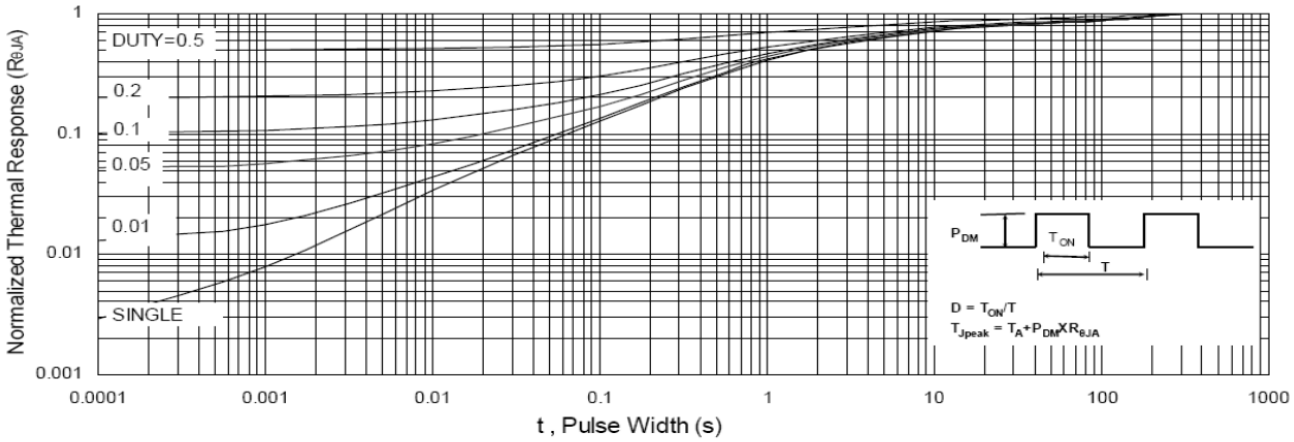


Fig.9 Normalized Maximum Transient Thermal Impedance

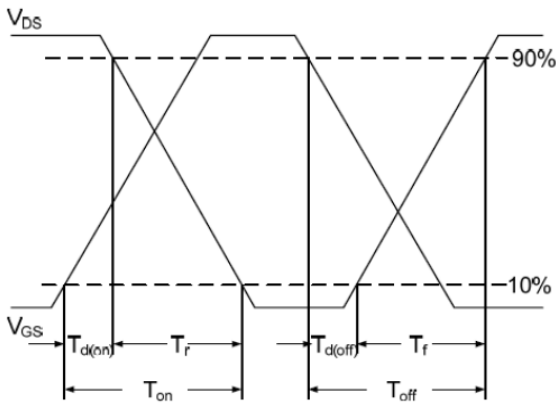


Fig.10 Switching Time Waveform

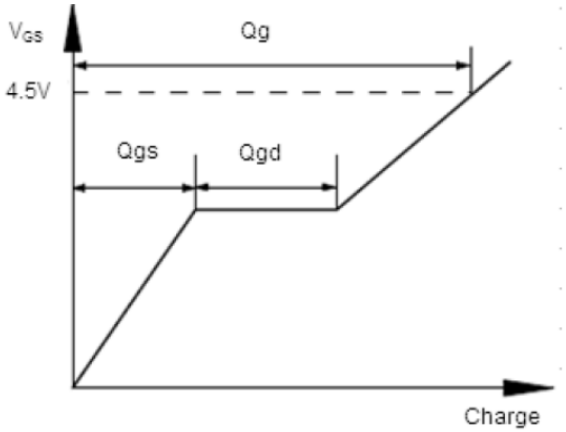


Fig.11 Gate Charge Waveform

CHARACTERISTIC CURVE (P-Ch)

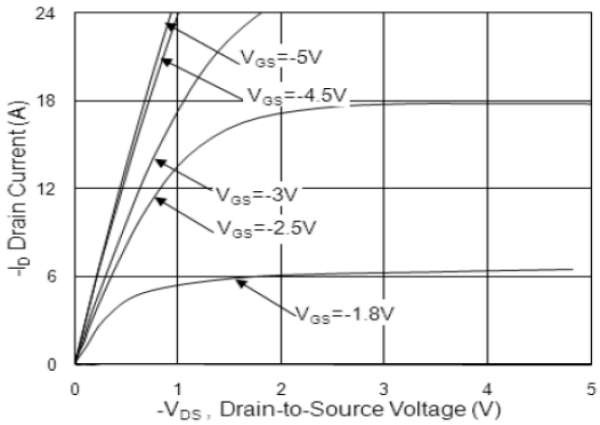


Fig.1 Typical Output Characteristics

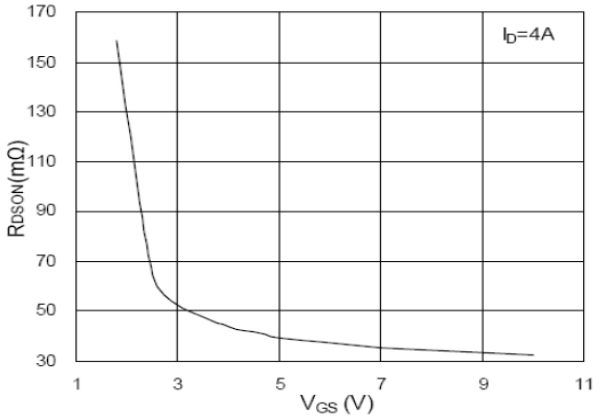
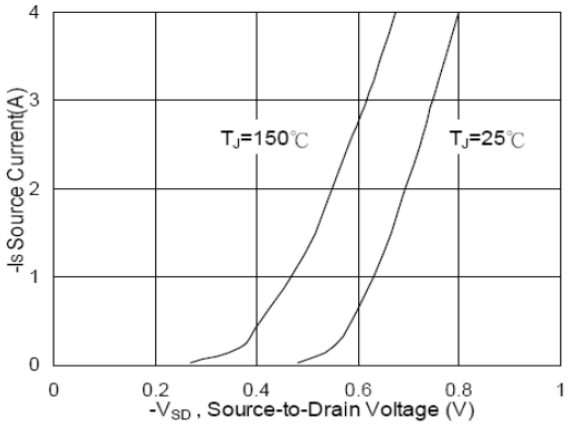


Fig.2 On-Resistance vs. Gate-Source



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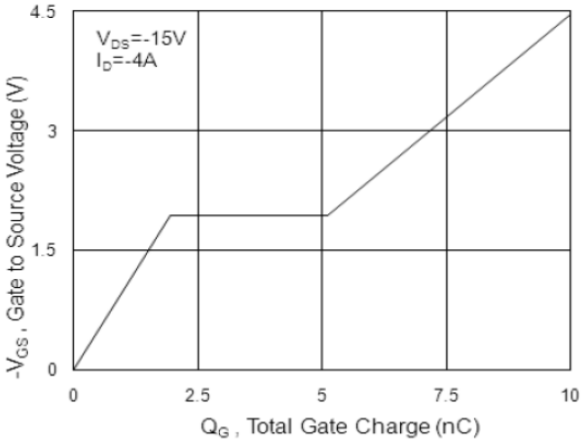


Fig.4 Gate-Charge Characteristics

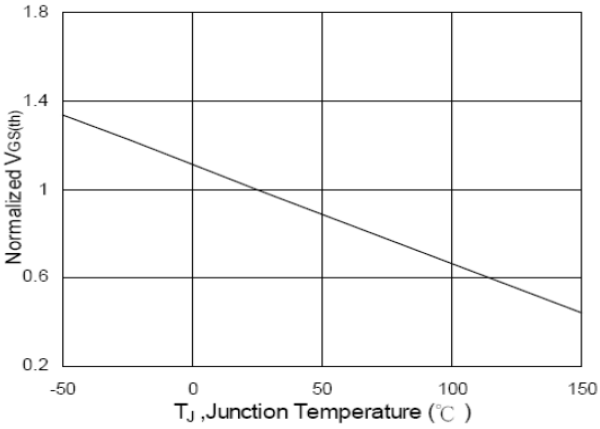


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

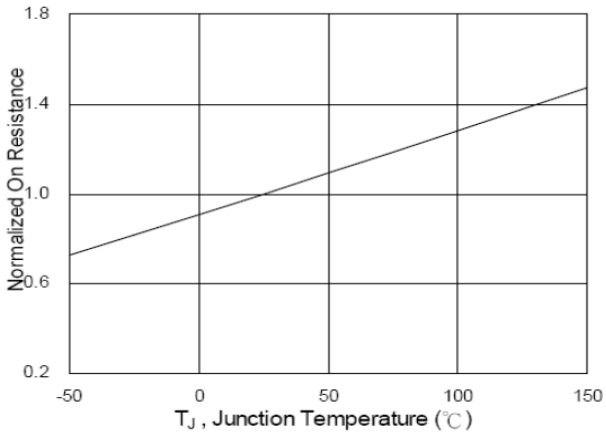


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVE (P-Ch)

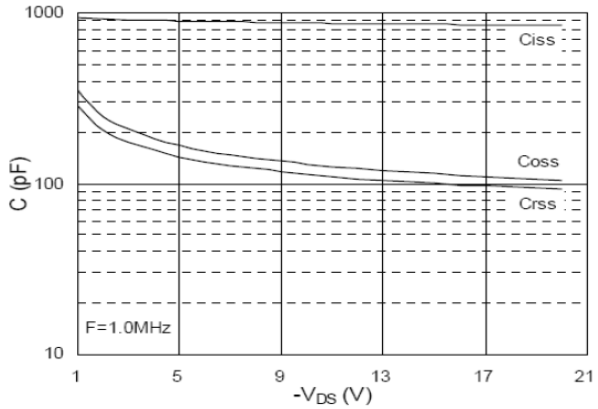
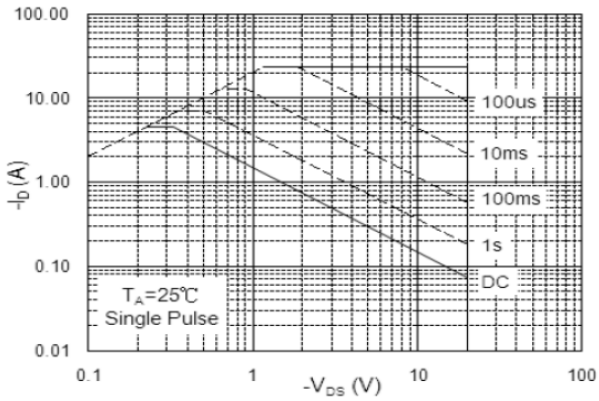


Fig.7 Capacitance



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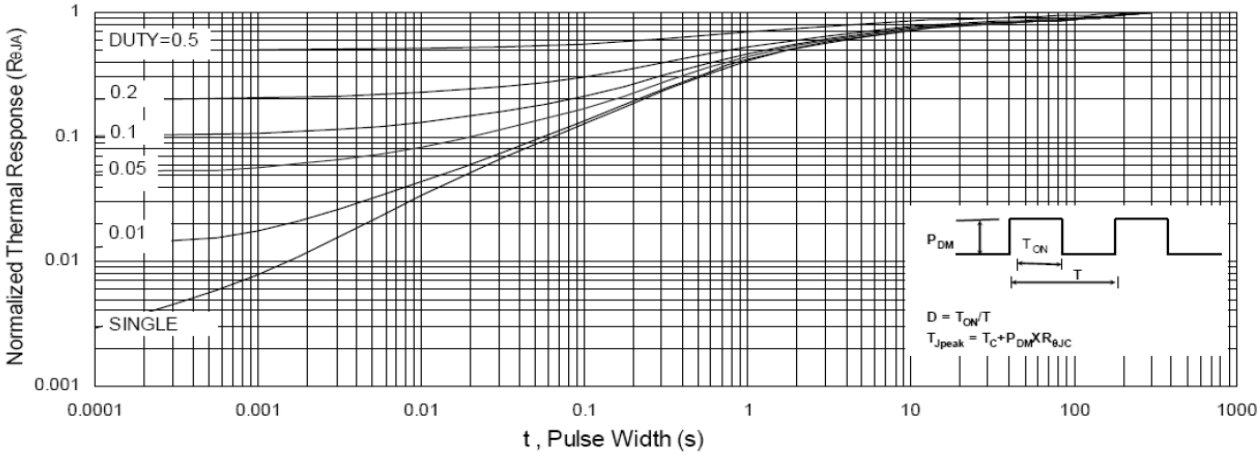

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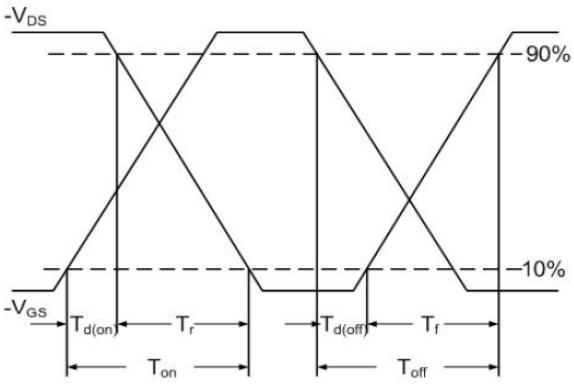

Fig.10 Switching Time Waveform

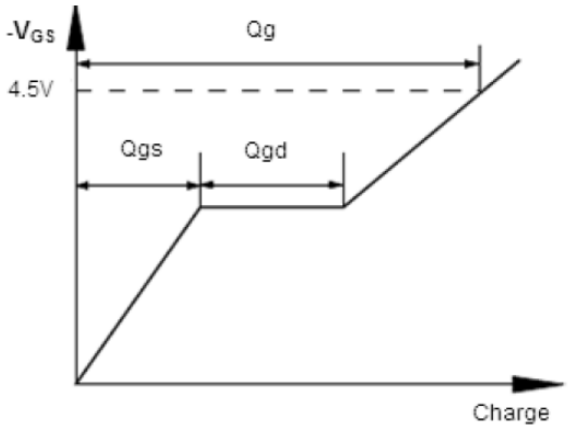

Fig.11 Gate Charge Waveform