Elektronische Bauelemente

SSG4N10E

4A, 100V, $R_{DS(ON)}$ 120mΩ

Dual-N Enhancement Mode Power MOSFET

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

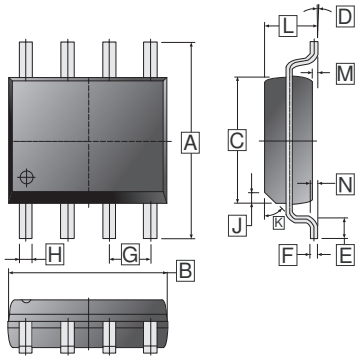
DESCRIPTION

The SSG4N10E provide the designer with the best Combination of fast switching, ruggedized device design, Ultra low on-resistance and cost-effectiveness.

FEATURES

- Low on-resistance
- Simple Drive Requirement
- Double-N MosFET Package

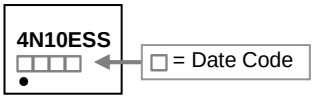
SOP-8



Dimensions in millimeters

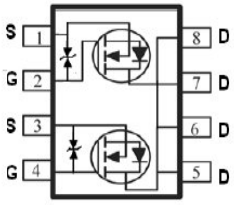
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

MARKING CODE



PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	3K	13' inch



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current@ V_{GS} =10V [1]	T_A = 25℃	I_D	4	A
	T_A = 70℃		3.1	
Pulsed Drain Current [2]		I_{DM}	15	A
Single Pulse Avalanche Energy [3]		EAS	9	mJ
Avalanche Current		I_{AS}	6	A
Power Dissipation@ T_A=25℃ [4]		P_D	1.5	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-ambient (Max.) [1]		$R_{\theta JA}$	85	℃ / W
Thermal Resistance Junction-Case (Max.) [1]		$R_{\theta JC}$	50	℃ / W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	3	V	V_{DS}=V_{GS}, I_D =250μA
Gate-Body Leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS}=80V,V_{GS}=0, T_J=25℃
		-	-	30		V_{DS}=80V$_{GS}$=0, T_J=85℃
Drain-Source On-Resistance [2]	$R_{DS(ON)}$	-	-	120	mΩ	V_{GS}=10V, I_D =4A
		-	-	135		V_{GS}=4.5V, I_D =3.5A
Gate Resistance	R_g	-	2.5	-	Ω	f=1.0MHz
Total Gate Charge (V_{GS}= 4.5V)	Q_g	-	6.1	-	nC	I_D= 4A V_{DS}= 30V V_{GS}= 10V
Total Gate Charge	Q_g	-	13	-		
Gate-Source Charge	Q_{gs}	-	2.2	-		
Gate-Drain (“Miller”) Charge	Q_{gd}	-	2.4	-		
Turn-On Delay Time	$T_{d(on)}$	-	10	-	nS	V_{DD}= 30V I_D= 1A V_{GEN}= 10V R_G= 6Ω R_L= 30Ω
Rise Time	T_r	-	7	-		
Turn-Off Delay Time	$T_{d(off)}$	-	22	-		
Fall Time	T_f	-	4	-		
Input Capacitance	C_{iss}	-	585	-	pF	V_{GS}=0V V_{DS}=30V f=1.0MHz
Output Capacitance	C_{oss}	-	36	-		
Reverse Transfer Capacitance	C_{rss}	-	20	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy [5]	EAS	4	-	-	mJ	V_{DD}= 25V, L=0.5mH, I_{AS}= 4A
Source-Drain Diode						
Continuous Source Current[1,6]	I_S	-	-	4	A	V_G = V_D=0V, Force Current
Pulsed Source Current[2,6]	I_{SM}	-	-	15	A	
Forward On Voltage [2]	V_{DS}	-	-	1.3	V	I_S=4A, V_{GS}=0V, T_J=25℃
Reverse Recovery Time	t_{rr}	-	25	-	nS	IF=4A, dI/dt=100A/μs, T_J=25℃
Reverse Recovery Charge	Q_{rr}	-	34	-	nC	

Notes:

1. Surface mounted on a 1 inch^2 FR-4 board with 2OZ copper. 135℃/W when mounted on Min. copper pad.
2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.
3. The EAS data shows Max. rating. The test condition is VDD=25V, VGS=10V, L=0.5mH, IAS=6A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

CHARACTERISTICS CURVE

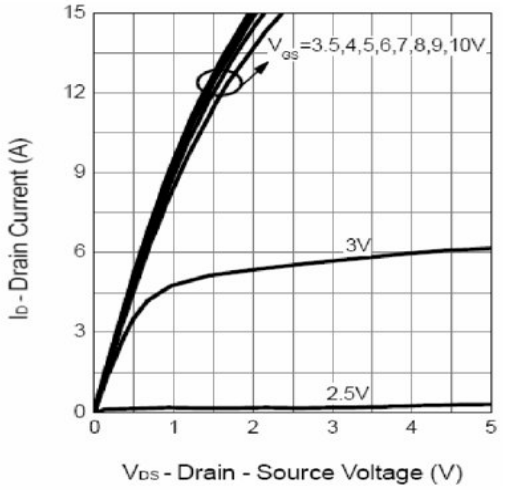


Fig 1. Typical Output Characteristics

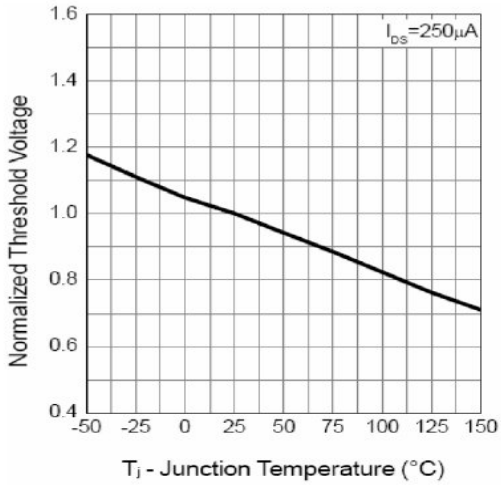


Fig 2. Gate Threshold Voltage

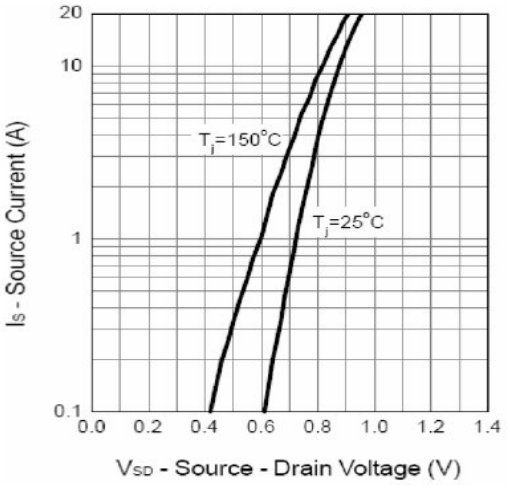


Fig 3. Typical Source-Drain Diode Forward Voltage

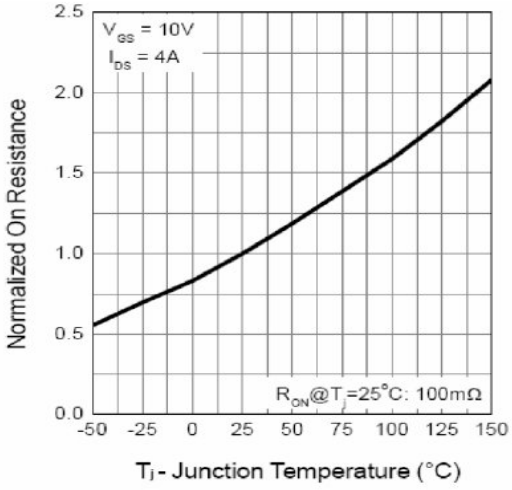


Fig 4. Normalized On-Resistance vs. Junction Temperature

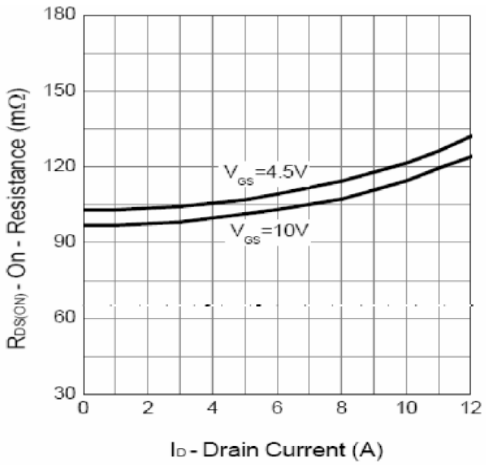


Fig 5. Typical On-Resistance vs. Drain Current

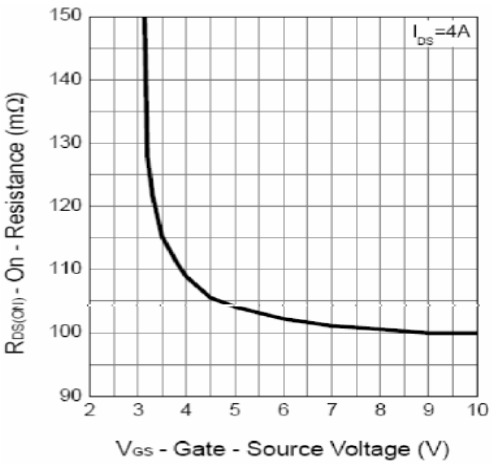


Fig 6. Typical On-Resistance vs. Gate Voltage

CHARACTERISTICS CURVE

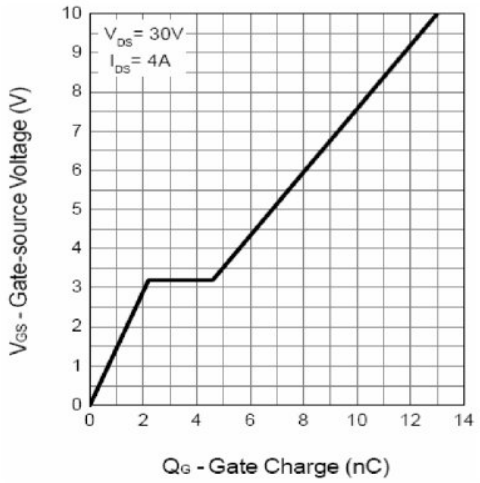


Fig 7. Gate Charge Characteristics

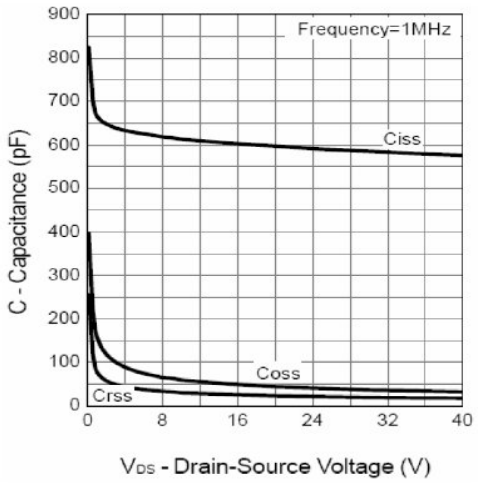


Fig 8. Typical Capacitance Characteristics

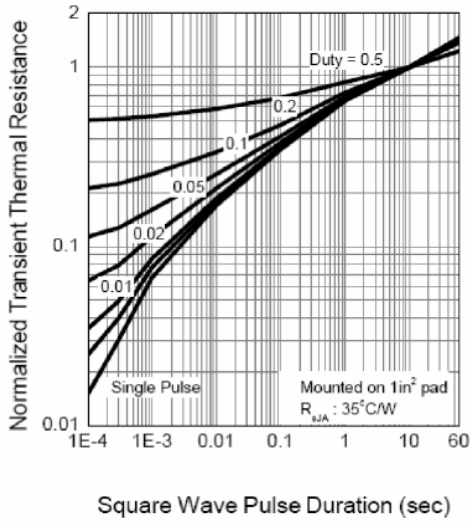


Fig 9. Thermal Transient Impedance

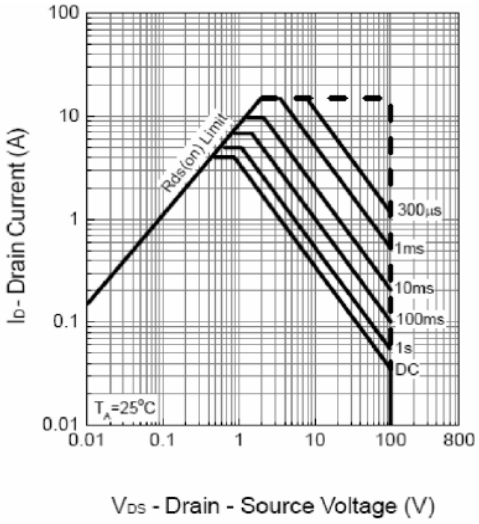


Fig 10. Maximum Safe Operating Area