

Features

- 39 dB Gain
- 31.5 dB, 0.5 dB steps, 6 Bit Digital Step Attenuator
- 36 dB MER, 64 QAM 39 Channels, 52 dBmV/ch.
- 8 V, 280 mA
- 3 dB Noise Figure
- Serial or Parallel Attenuator Control
- Differential Input and Output
- Low Harmonics
- Power Down Mode
- Lead-Free 7 mm PQFN-48LD
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAAM-011122 is an integrated 2 stage differential amplifier with embedded digital step attenuator (DSA). This part is intended for CATV Reverse Path applications. The module provides excellent linearity and high output power with greater than 30 dB MER for 64 QAM modulation with 39 channels and 52 dBmV per channel. Gain in the minimum attenuation state is typically 39 dB. The internal DSA offers 31.5 dB attenuation range with 0.5 dB steps. The module also provides power down function for each of the amplifier stages.

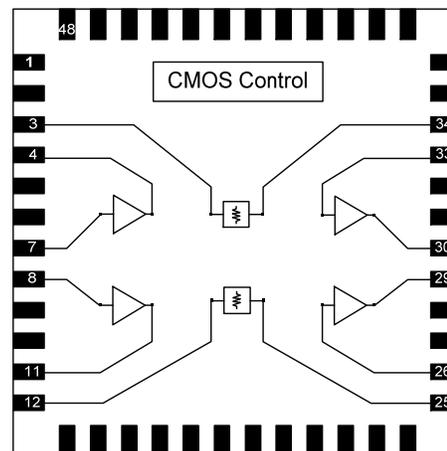
The part is packaged in a lead-free 7 mm PQFN package.

Ordering Information^{1,2}

Part Number	Package
MAAM-011122-TR1000	1000 piece reel
MAAM-011122-TR3000	3000 piece reel
MAAM-011122-001SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration³

Pin No.	Description	Pin No.	Description
1	Latch Enable	30	Stage 2 Output (+)
3	Attenuator Input (+)	32	Stage 2 Feedback(+)
4	Stage 1 Output (+)	33	Stage 2 Input (+)
6	Stage 1 Feedback(+)	34	Attenuator Output (+)
7	Stage 1 Input (+)	36	DSA Serial Output
8	Stage 1 Input (-)	37	Power Up Select 2
9	Stage 1 Feedback(-)	38	Power Up Select 1
11	Stage 1 Output (-)	39	V _{DD} CMOS Controller
12	Attenuator Input (-)	40	Attenuator Bit 5 (16 dB)
16	Enable Stage 1	41	Attenuator Bit 4 (8 dB)
18	Stage 1 Bias Voltage	42	Attenuator Bit 3 (4 dB)
19	Stage 2 Bias Voltage	43	Attenuator Bit 2 (2 dB)
21	Enable Stage 2	44	Attenuator Bit 1 (1 dB)
25	Attenuator Output (-)	45	Attenuator Bit 0 (0.5 dB)
26	Stage 2 Input (-)	46	Parallel/Serial Select
27	Stage 2 Feedback(-)	47	Clock
29	Stage 2 Output (-)	48	Serial Input
		49	RF and DC Ground ⁴

3. All pins not listed in the table are "No Connection" and should be left unconnected.
4. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Differential CATV Variable Gain Amplifier 5 - 300 MHz

Rev. V1

Electrical Specifications:

$T_A = 25^\circ\text{C}$, $V_{CC} = +8$ Volts, Minimum attenuation state, $Z_0 = 75 \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	Max. Gain State @ 100 MHz, -29 dBm Pin	dB	—	39	—
Gain Slope	Positive tilt from 5 - 250 MHz	dB	—	1.2	—
Noise Figure ⁵	—	dB	—	3.0	—
Input Return Loss	—	dB	—	22	—
Output Return Loss	—	dB	—	22	—
Reverse Isolation	—	dB	—	50	—
Attenuation Range	100 MHz relative to max. attenuation gain, -29 dBm Pin	dB	30	31.5	33
64 QAM MER ⁶	39 Channels (5-250 MHz), 52 dBmV/Ch. Single Channel (8-200 MHz), 72 dBmV/Ch. Single Channel (250 MHz), 71 dBmV/Ch. 16 Channels (5-200 MHz), 57 dBmV/Ch.	dB	— 30 30 30	36 35 35 34	—
P1dB	—	dBm	—	27	—
OIP2	2-tone, 12 dBm/tone, 1 MHz tone spacing, 200 MHz	dBm	—	70	—
OIP3	2-tone, 12 dBm/tone, 1 MHz tone spacing, 200 MHz	dBm	—	42	—
T_{ON} , T_{OFF}	50% Control to 90 / 10 % RF	ns	—	400	—
I_{CC}	EN1 = EN2 = 5 V	mA	—	280	315
I_{CC_OFF}	EN1 = EN2 = 0 V	mA	—	3	10

5. Includes Balun Loss

6. Modulation error ratio each channel 64 QAM 5.12 MS/s

Absolute Maximum Ratings^{7,8,9}

Parameter	Absolute Maximum
RF Input Power	-8 dBm
Voltage	10 volts
Operating Temperature	-40°C to +100°C
Junction Temperature ¹⁰	+150°C
Storage Temperature	-65°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.

8. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.

9. Operating at nominal conditions with $T_J \leq 150^\circ\text{C}$ will ensure $MTTF > 1 \times 10^6$ hours.

10. Junction Temperature (T_J) = $T_C + \Theta_{jc} * (V * I)$
Typical thermal resistance (Θ_{jc}) = 8.85° C/W.

a) For $T_C = 25^\circ\text{C}$,

$T_J = 44^\circ\text{C}$ @ +8 V, 275 mA

b) For $T_C = 100^\circ\text{C}$,

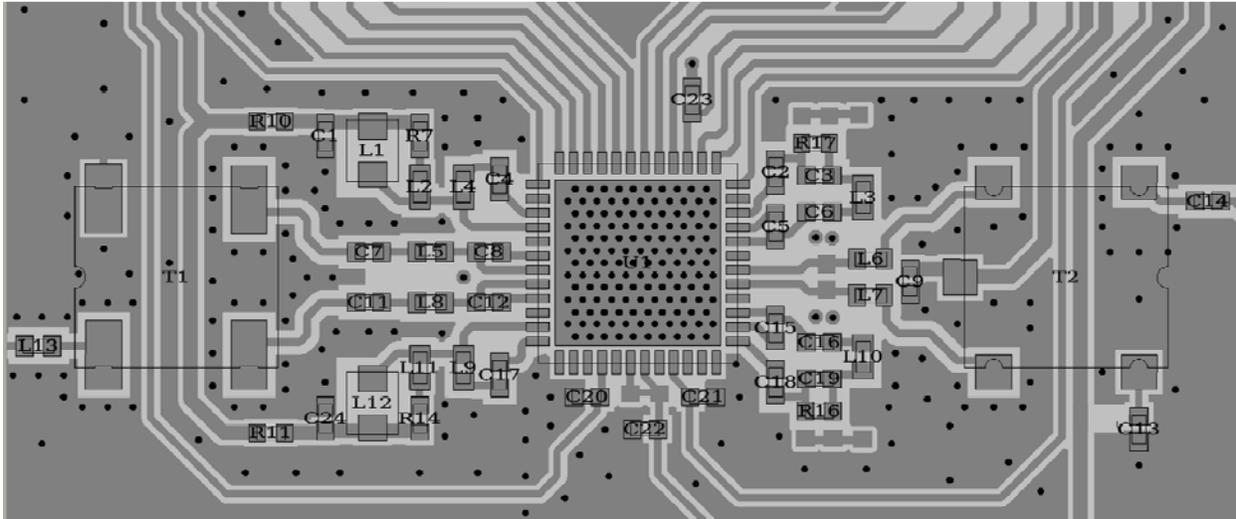
$T_J = 119^\circ\text{C}$ @ +8 V, 275 mA

Truth Table¹¹

B5	B4	B3	B2	B1	B0	Attenuation (dB)
1	1	1	1	1	1	Minimum
1	1	1	1	1	0	0.5
1	1	1	1	0	1	1
1	1	1	0	1	1	2
1	1	0	1	1	1	4
1	0	1	1	1	1	8
0	1	1	1	1	1	16
0	0	0	0	0	0	31.5

11. Logic "0" = 0 V to +0.8 V \pm 0.2 V,
Logic "1" = +2 V to +5 V \pm 0.2 V

PCB Layout¹²



12. 136 vias underneath the IC of 0.241 mm in diameter.

Parts List¹³

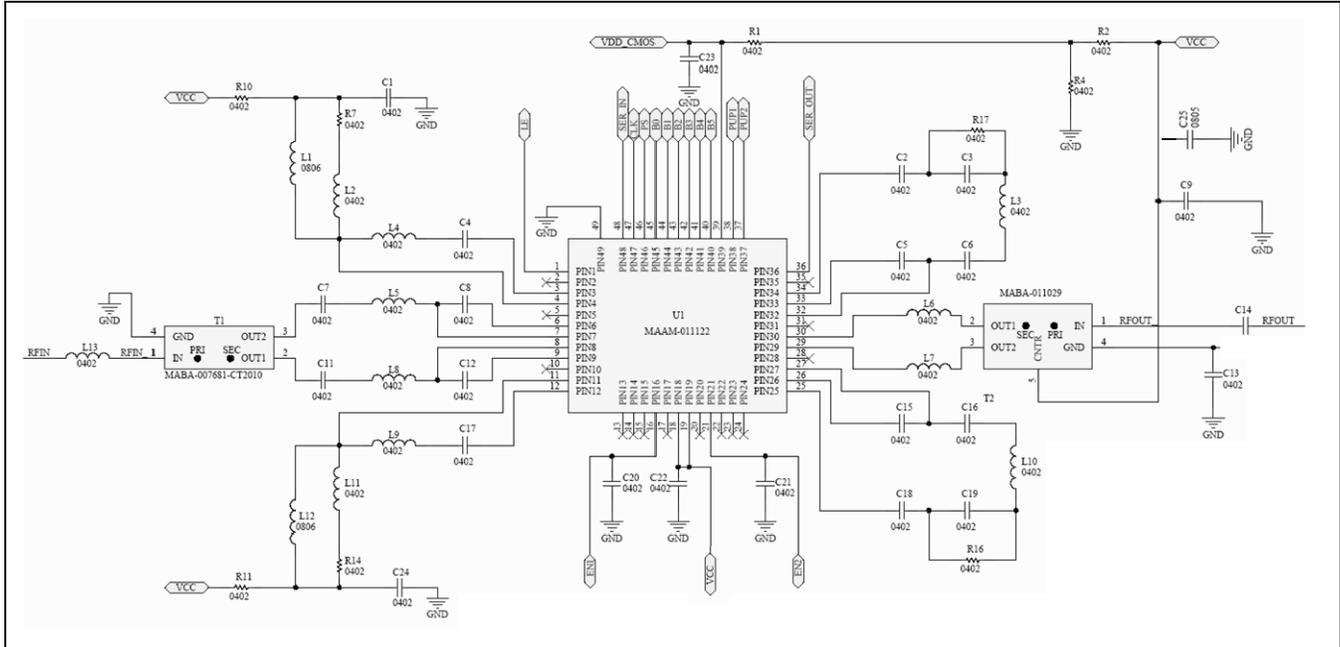
Part	Value	Case Style
C1, C9, C13, C20, C21, C22, C23, C24	0.1 μ F	0402
C2, C4, C5, C6, C7, C8, C11, C12, C15, C16, C17, C18	0.01 μ F	0402
C3, C19	47 pF	0402
C14	2200 pF	0402
C25	1 μ F	0805
L1, L12 ¹⁴	47 μ H	0806
L2, L11 ¹⁵	250 nH	0402
L3, L10	18 nH	0402
L4, L9	10 nH	0402
L5, L8	27 nH	0402
L6, L7	30 nH	0402
L13	5.6 nH	0402
R1, R10, R11	0 Ω	0402
R2	3 k Ω	0402
R4	5 k Ω	0402
R7, R14	249 Ω	0402
R16, R17	27 Ω	0402

13. The baluns are M/A-COM Technology Solutions parts, T1 is MABA-007681-CT2010 and T2 is MABA-011029.

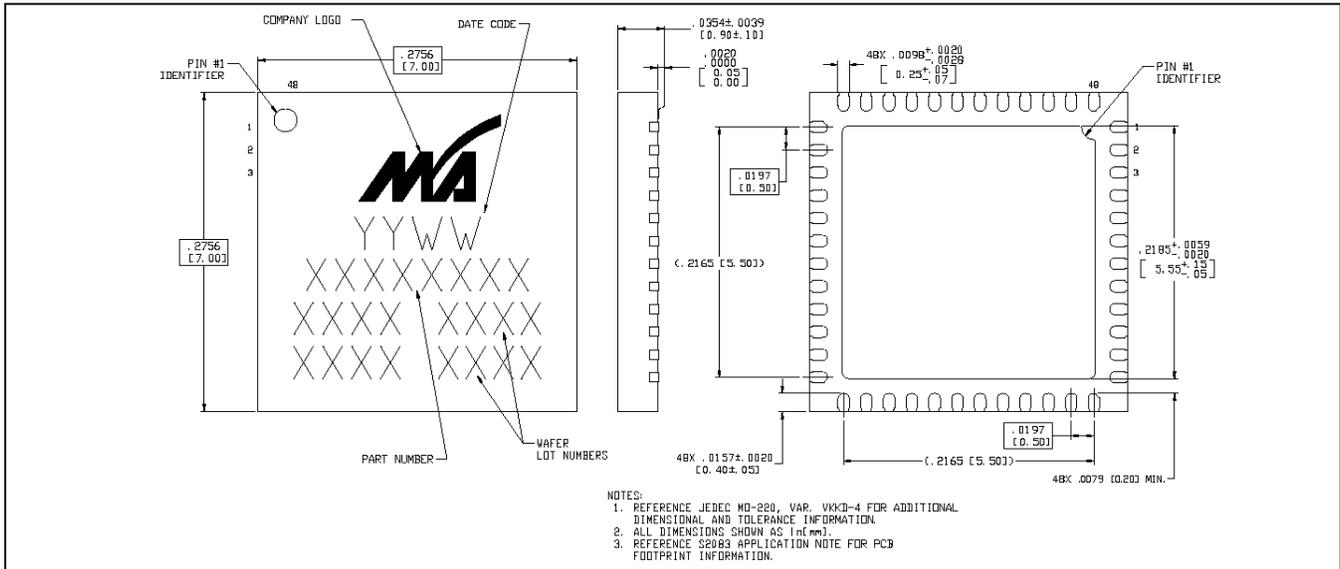
14. 47 μ H inductor is Murata LQH2MCN470K02L.

15. 250 nH inductor is Coilcraft 0402AF-251XJLU.

Application Schematic



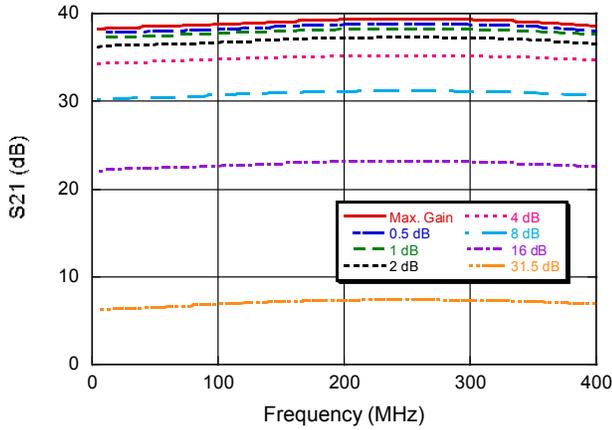
Lead-Free 7 mm 48-lead PQFN



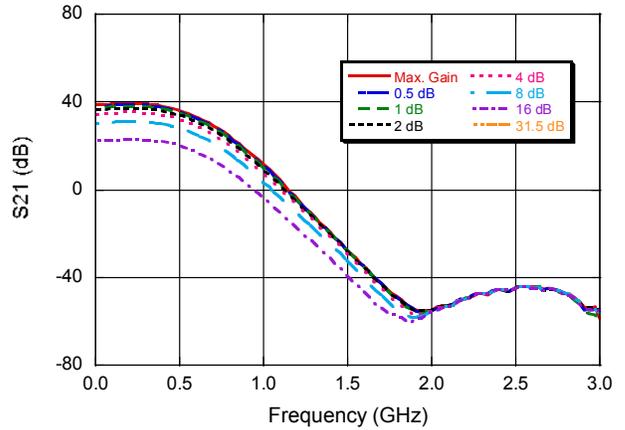
† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAuAg.

Typical Performance Curves:

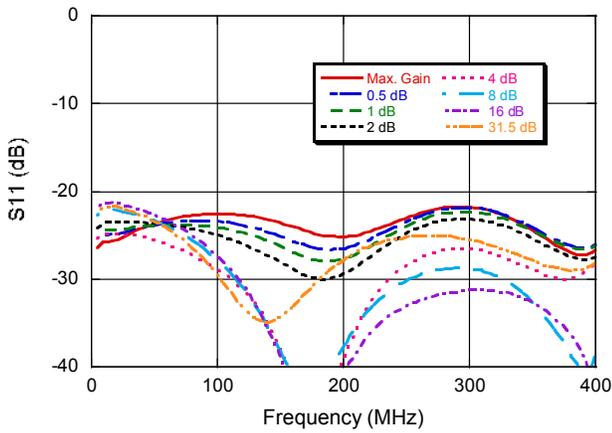
Gain



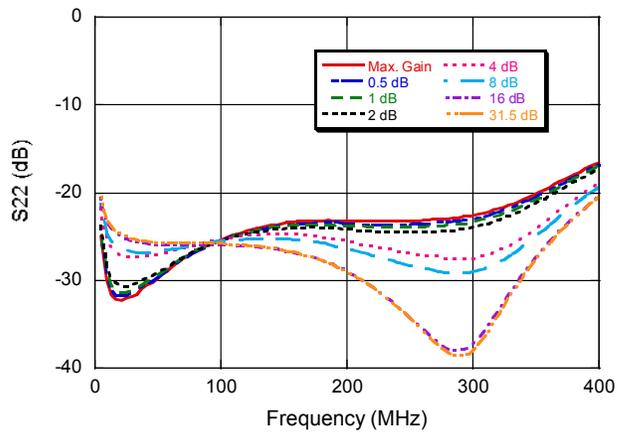
Gain - Wideband



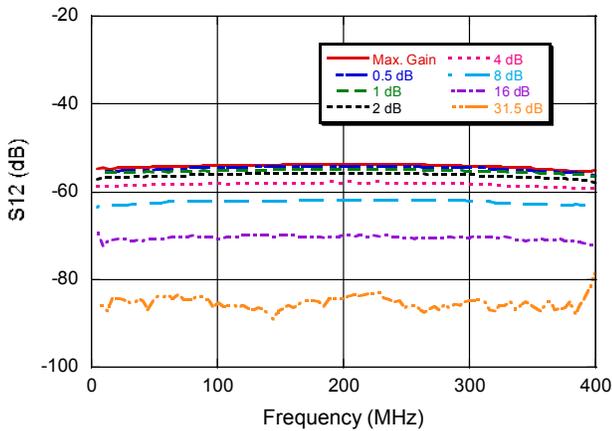
Input Return Loss



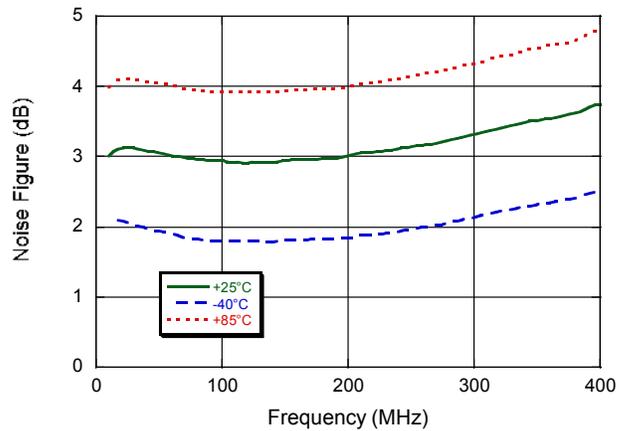
Output Return Loss



Reverse Isolation

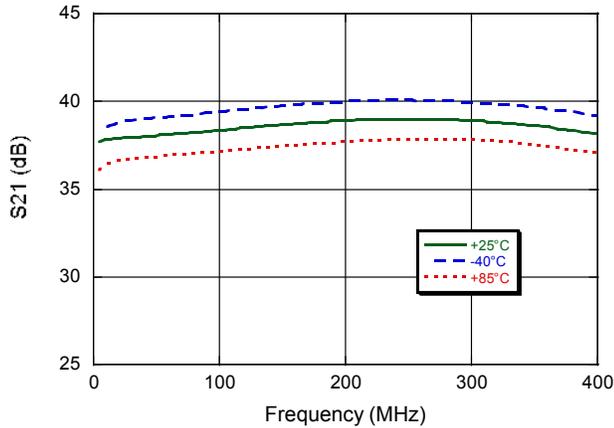


Noise Figure

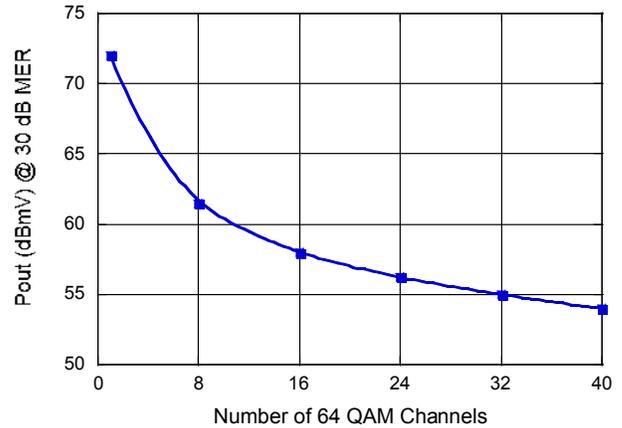


Typical Performance Curves:

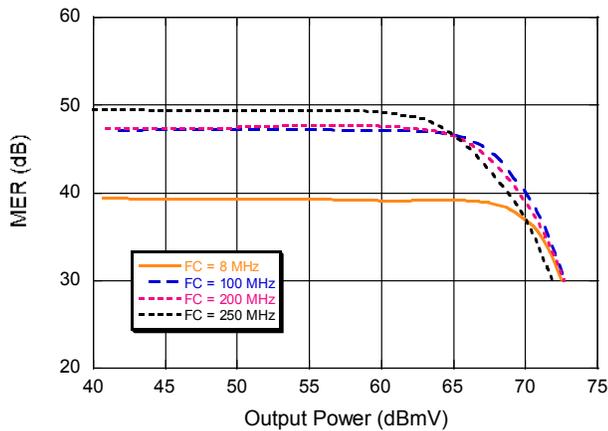
Gain



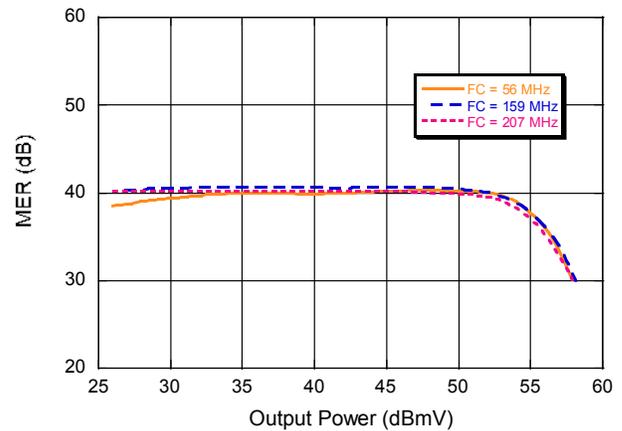
P_{OUT} @ 30 dB MER



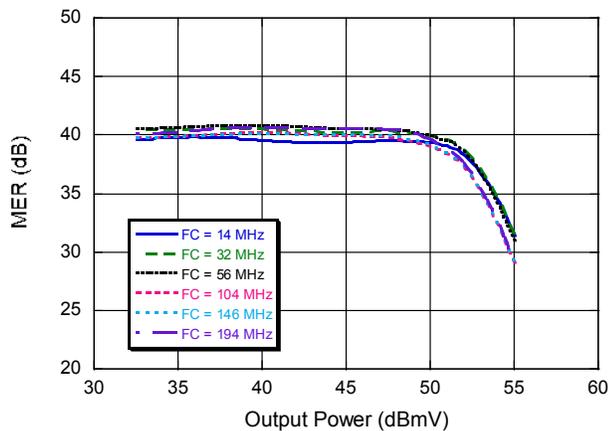
Modulation Error Ratio (64 QAM, single channel)



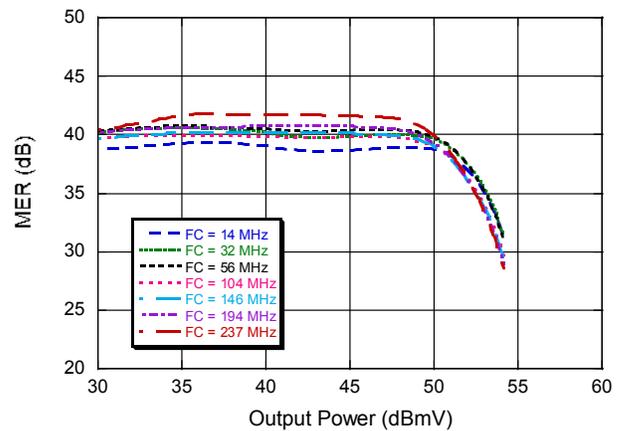
Modulation Error Ratio (64 QAM, 16 channel)



Modulation Error Ratio (64 QAM, 32 channel)



Modulation Error Ratio (64 QAM, 40 channel)



Functionality

Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	Constant High	Direct Parallel
0	Pulsed	Latched Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with MSB first. After shifting in the 6 bit word, bringing LE high will set the attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is the SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled and the serial input register is loaded asynchronously with parallel digital inputs.

Direct Parallel Mode

The parallel mode is enabled when P/S is set to low. In the direct parallel mode, the attenuator is controlled by the parallel control inputs directly. The LE must be at logic high to control the attenuator in this mode.

Latched Parallel Mode

In the latched parallel mode, the parallel control inputs will be buffered by registers, and loaded to the outputs when LE is high. The outputs shall not change states when LE is low.

Power-up States

The power-up (PUP) states will work in both serial and parallel modes, and initiate the attenuator according to the PUP truth table. During power up, the digital inputs shall be held constant for at least 1 μ s after V_{CC} reaches 90% of final value. For serial mode, the PUP states will only work when LE is held low. The PUP state shall be locked out after the first LE pulse. Proper operation of power up states requires fast rise time (<200 ns) for $V_{DD-CMOS}$.

Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

PUP Truth Table

Inputs				Gain Relative to Max. Gain	Notes
PS	LE	PUP2	PUP1		
0	0	0	0	-31.5 dB	Parallel Mode
0	0	0	1	-24 dB	
0	0	1	0	-16 dB	
0	0	1	1	0 dB	
0	1	X	X	0 to -31.5 dB (Set B0 - B5)	Serial Mode
1	0	X	X	0 to -31.5 dB (Set B0 - B5)	
1	1	X	X	No Definition	

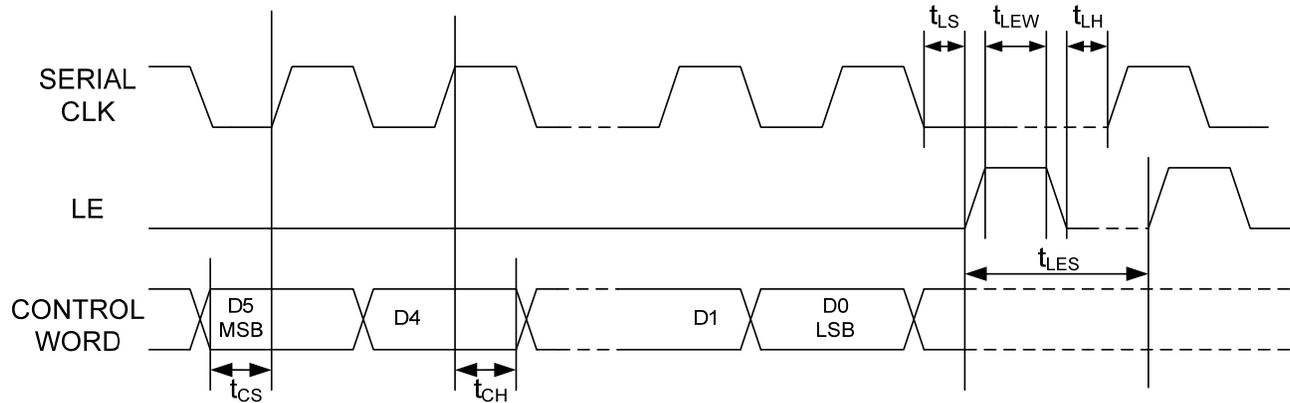
Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+85°C	
t _{SCK}	Min. Serial Clock Period	100	100	100	ns
t _{CS}	Min. Control Set-up Time	20	20	20	ns
t _{CH}	Min. Control Hold Time	20	20	20	ns
t _{LS}	Min. LE Set-up Time	10	10	10	ns
t _{LEW}	Min. LE Pulse Width	10	10	10	ns
t _{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t _{LES}	Min. LE Pulse Spacing	630	630	630	ns

Functionality

Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Serial Input Interface Timing Diagram



Parallel Control Word

