

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD50N03 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

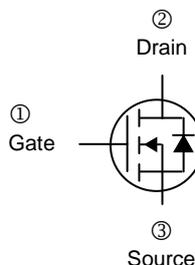
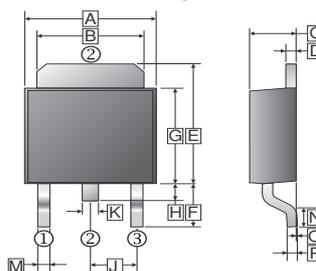
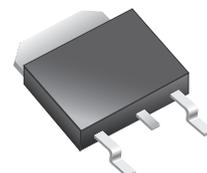
MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30	REF.
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}=10V$ ¹	I_D	$T_C=25^\circ\text{C}$	51
		$T_C=100^\circ\text{C}$	36
		$T_A=25^\circ\text{C}$	12.4
		$T_A=70^\circ\text{C}$	10.3
Pulsed Drain Current ²	I_{DM}	120	A
Single Pulse Avalanche Energy ³	E_{AS}	130	mJ
Single Pulse Avalanche Current	I_{AS}	34	A
Total Power Dissipation ⁴	P_D	41.7	W
$T_C=25^\circ\text{C}$			
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Maximum Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	3	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	62	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions	
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS}=0, I_D=250\mu A$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$	
Forward Transconductance	g_{fs}	-	42	-	S	$V_{DS}=5V, I_D=30A$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}= \pm 20V$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ C$	-	-	1	μA	$V_{DS}=24V, V_{GS}=0$
		$T_J=55^\circ C$	-	-	5		
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	-	9	m Ω	$V_{GS}=10V, I_D=30A$	
		-	-	13.5		$V_{GS}=4.5V, I_D=15A$	
Total Gate Charge	Q_g	-	10.6	-	nC	$I_D=15A$ $V_{DS}=15V$ $V_{GS}=4.5V$	
Gate-Source Charge	Q_{gs}	-	4.2	-			
Gate-Drain ("Miller") Change	Q_{gd}	-	4	-			
Turn-on Delay Time	$T_{d(on)}$	-	6.4	-	nS	$V_{DD}=15V$ $I_D=15A$ $V_{GS}=10V$ $R_D=3.3 \Omega$	
Rise Time	T_r	-	70.6	-			
Turn-off Delay Time	$T_{d(off)}$	-	22.4	-			
Fall Time	T_f	-	8	-			
Input Capacitance	C_{iss}	-	1127	-	pF	$V_{GS}=0$ $V_{DS}=15V$ $f=1.0MHz$	
Output Capacitance	C_{oss}	-	194	-			
Reverse Transfer Capacitance	C_{rss}	-	77	-			
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy ⁵	E_{AS}	45	-	-	mJ	$V_{DD}=25V, L=0.1mH, I_{AS}=20A$	
Source-Drain Diode							
Continuous Source Current ^{1,6}	I_S	-	-	51	A	$V_G = V_D=0, \text{Force Current}$	
Pulsed Source Current ^{2,6}	I_{SM}	-	-	120	A		
Diode Forward Voltage ²	V_{SD}	-	-	1	V	$I_S=1A, V_{GS}=0$	
Reverse Recovery Time	T_{rr}	-	12	-	nS	$I_F=30A, di/dt=100A/\mu s$ $T_J=25^\circ C$	
Reverse Recovery Charge	Q_{rr}	-	3.7	-	nC		

Notes:

- The data tested by surface mounted on a 1 inch2 FR-4 board with 20Z copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=34A$.
- The power dissipation is limited by $150^\circ C$ junction temperature.
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and IDM , in real applications, should be limited by total power dissipation

CHARACTERISTIC CURVES

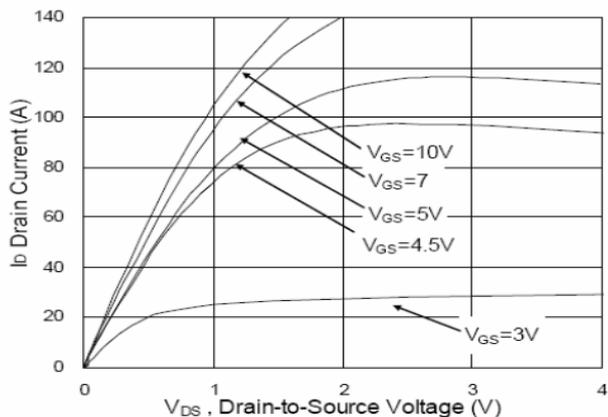


Fig.1 Typical Output Characteristics

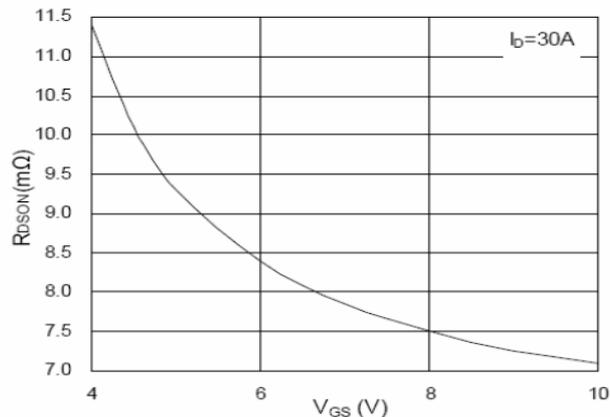


Fig.2 On-Resistance vs. Gate-Source

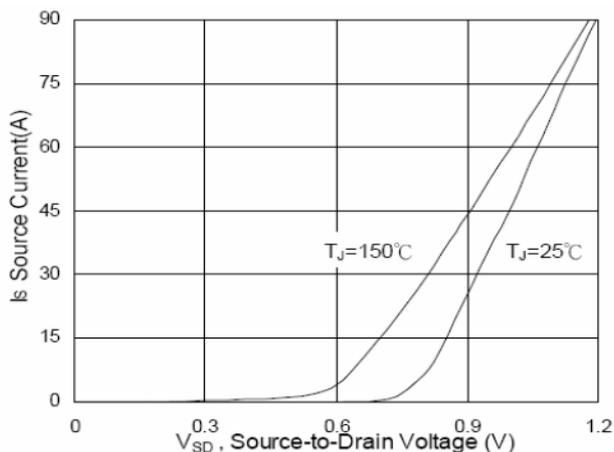


Fig.3 Forward Characteristics of Reverse

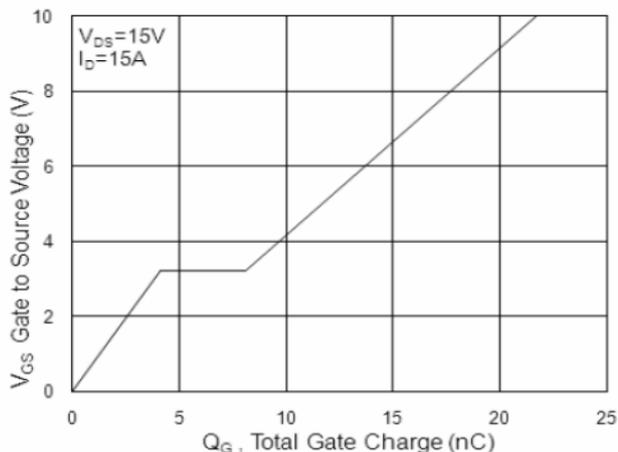


Fig.4 Gate-Charge Characteristics

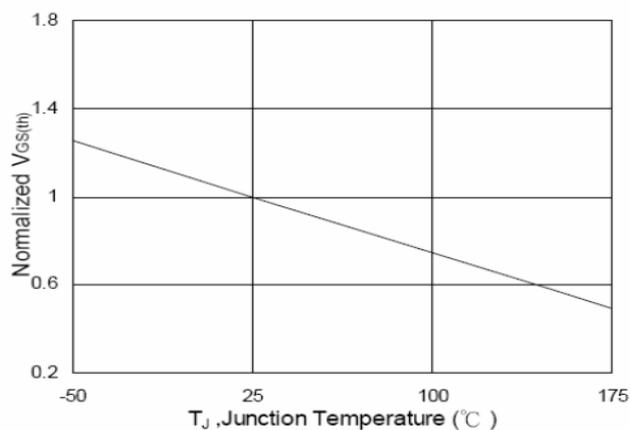


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

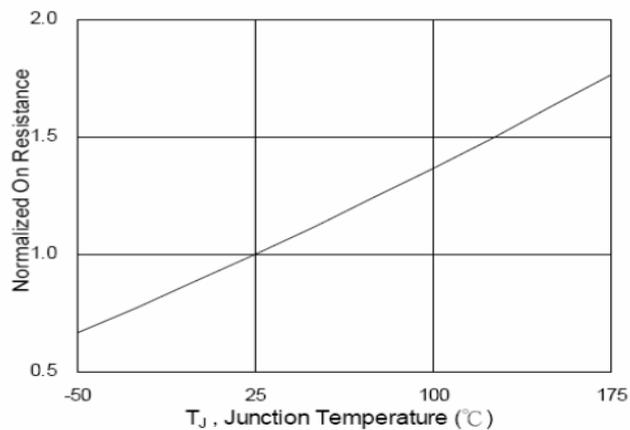


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

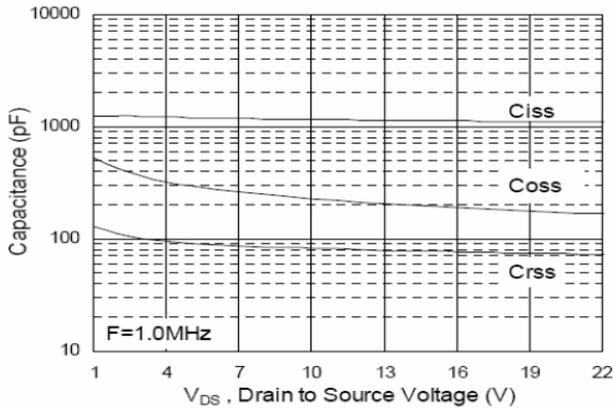


Fig.7 Capacitance

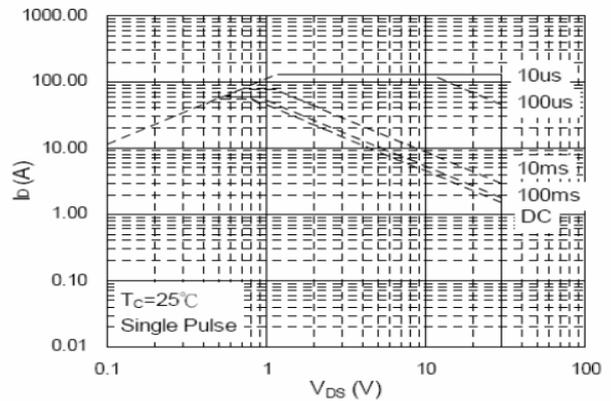


Fig.8 Safe Operating Area

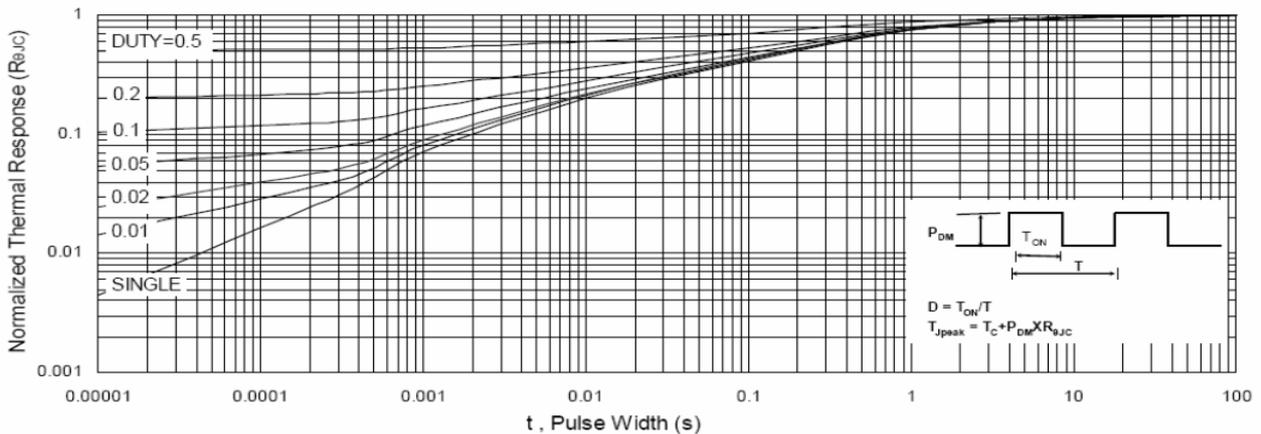


Fig.9 Normalized Maximum Transient Thermal Impedance

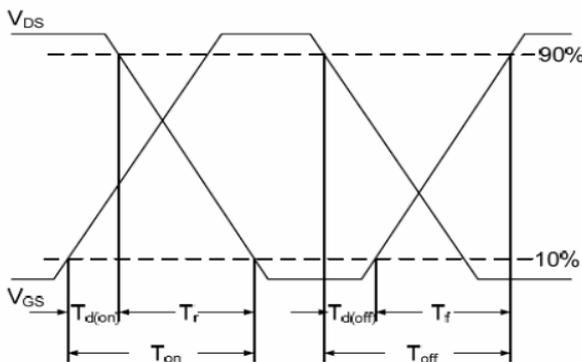


Fig.10 Switching Time Waveform

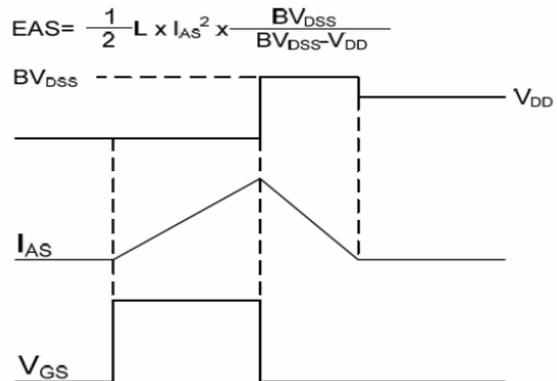


Fig.11 Unclamped Inductive Switching Waveform