

RoHS Compliant Product
A suffix of "-C" specifies halogen free

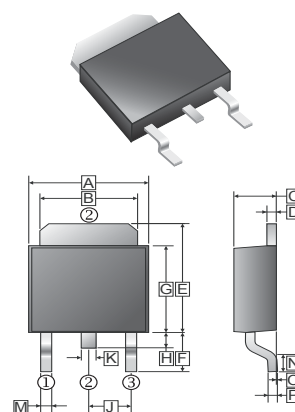
DESCRIPTION

These miniature surface mount MOSFETs utilize high cell density process. Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Miniature TO-252 surface mount package saves board space.
- High power and current handling capability.
- Extended V_{GS} range (± 25) for battery pack applications.

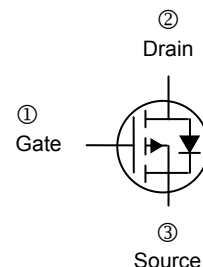
TO-252(D-Pack)



PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13' inch

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30 REF.	
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current @ $T_A=25^\circ\text{C}$ ¹	I_D	-44	A
Pulsed Drain Current ²	I_{DM}	-150	A
Continuous Source Current (Diode Conduction) ¹	I_S	-48	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$ ¹	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	$^\circ\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	40	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3	$^\circ\text{C} / \text{W}$

Notes :

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

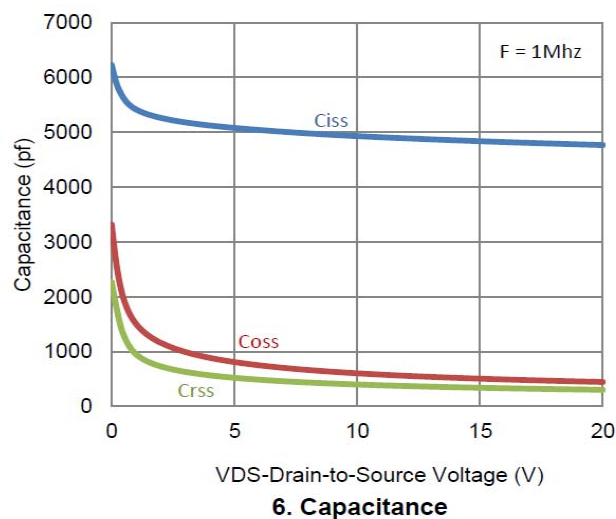
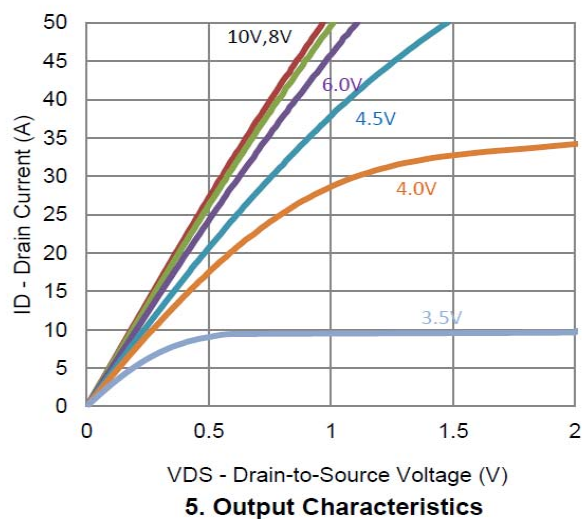
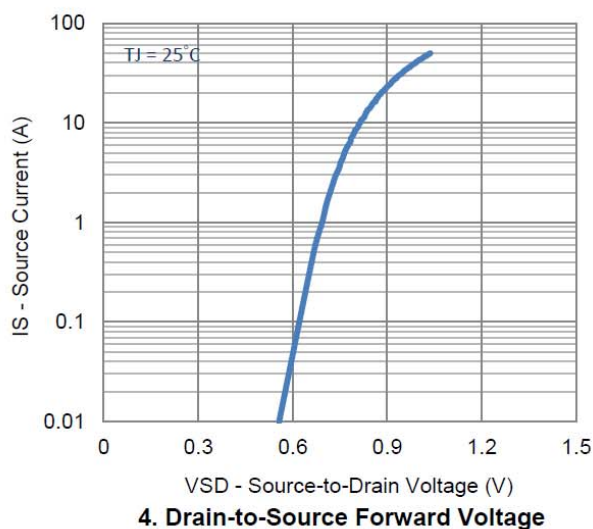
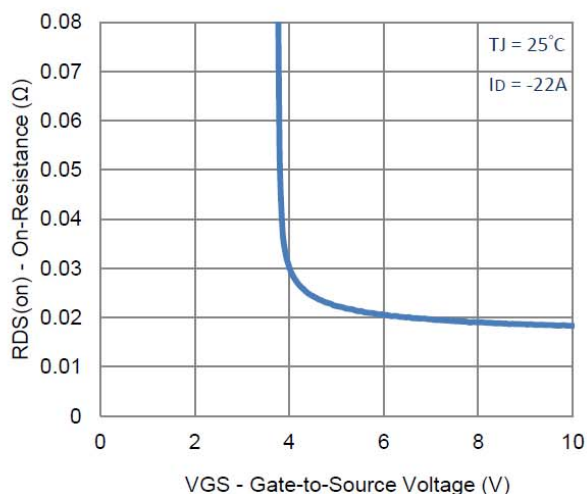
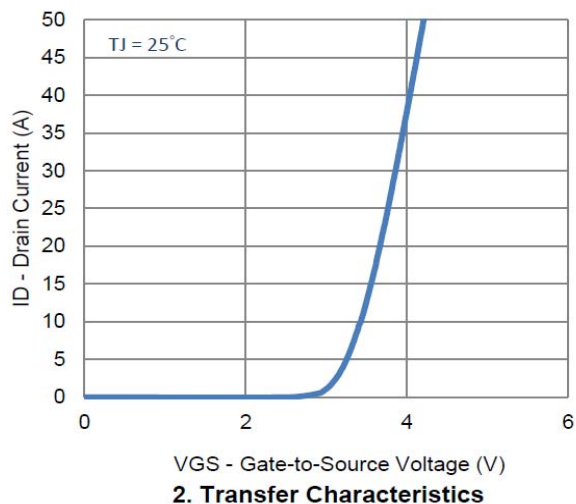
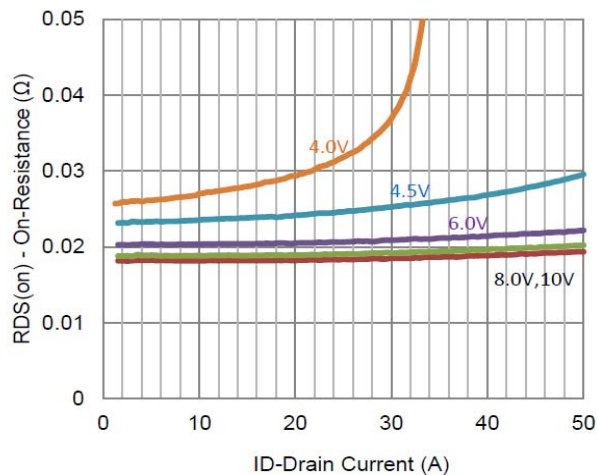
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0V$, $V_{GS} = \pm 20V$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -48V$, $V_{GS} = 0V$
		-	-	-10		$V_{DS} = -48V$, $V_{GS} = 0V$, $T_J = 55^\circ C$
On-State Drain Current ¹	$I_{D(on)}$	-20	-	-	A	$V_{DS} = -5V$, $V_{GS} = -10V$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	17	m Ω	$V_{GS} = -10V$, $I_D = -22A$
		-	-	23		$V_{GS} = -4.5V$, $I_D = -22A$
Forward Transconductance ¹	g_{fs}	-	8	-	S	$V_{DS} = -15V$, $I_D = -22A$
Diode Forward Voltage	V_{SD}	-	-0.9	-	V	$I_S = -24 A$, $V_{GS} = 0 V$
Dynamic ²						
Input Capacitance	C_{iss}	-	4654	-	pF	$V_{GS} = 0$ $V_{DS} = -15V$ $f = 1MHz$
Output Capacitance	C_{oss}	-	526	-		
Reverse Transfer Capacitance	C_{rss}	-	347	-		
Total Gate Charge	Q_g	-	83	-	nC	$V_{DS} = -30V$ $V_{GS} = -10V$ $I_D = -22A$
Gate-Source Charge	Q_{gs}	-	8	-		
Gate-Drain Charge	Q_{gd}	-	20	-		
Turn-on Delay Time	$T_{d(on)}$	-	11	-	nS	$V_{DD} = -30V$ $I_D = -22A$ $V_{GEN} = -10 V$ $R_L = 1.4\Omega$ $R_G = 6\Omega$
Rise Time	T_r	-	16	-		
Turn-off Delay Time	$T_{d(off)}$	-	113	-		
Fall Time	T_f	-	42	-		

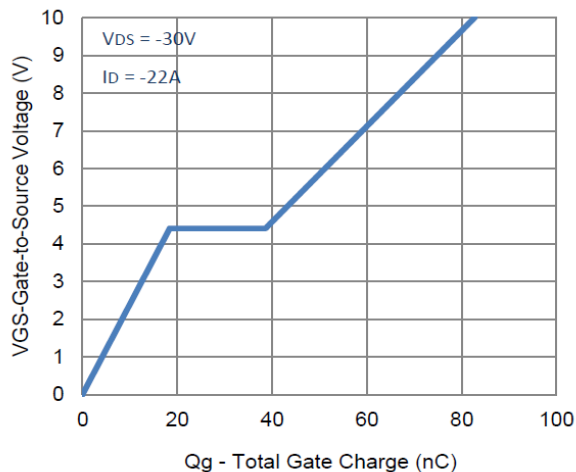
Notes:

1. Pulse test : Pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.

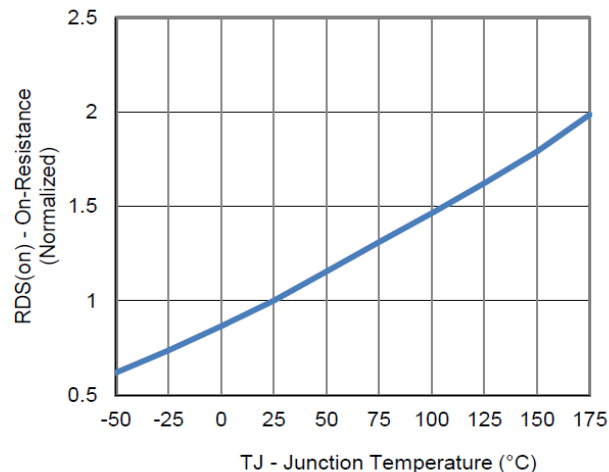
CHARACTERISTIC CURVE



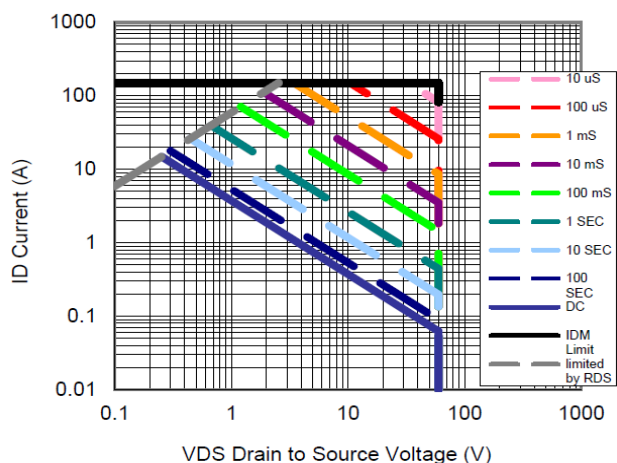
CHARACTERISTIC CURVE



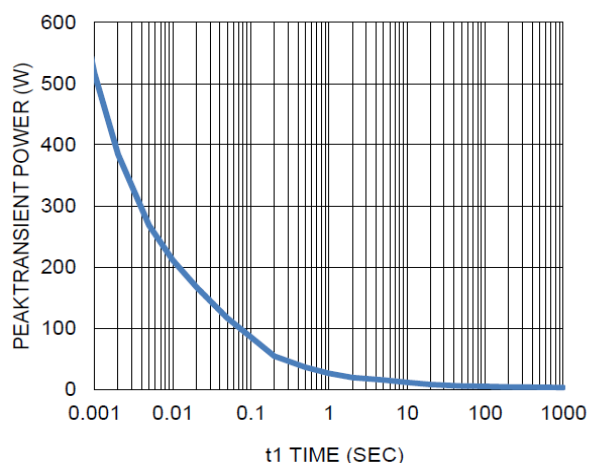
7. Gate Charge



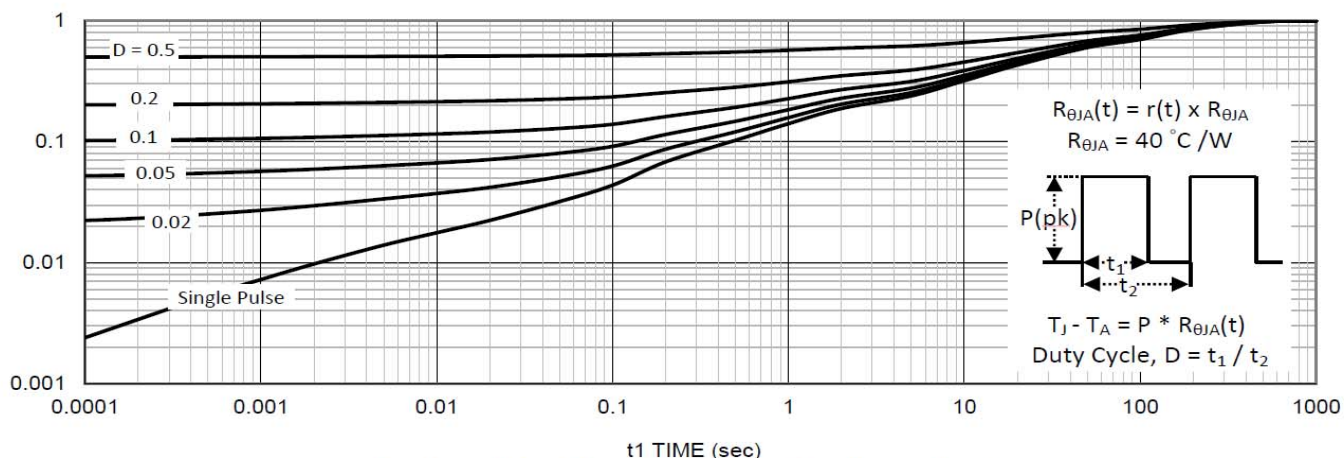
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area



10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient