

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSD80N03 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

MARKING

80N03

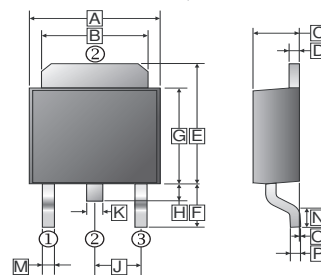
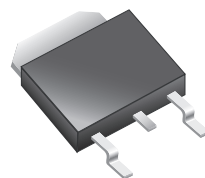


Date Code

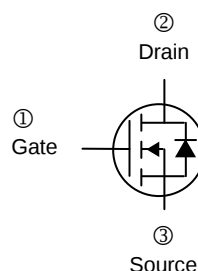
PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30 REF.	
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$V_{GS}=10V, T_C=25^\circ\text{C}$	I_D	80	A
	$V_{GS}=10V, T_C=100^\circ\text{C}$		57	A
Pulsed Drain Current ²		I_{DM}	160	A
Total Power Dissipation ⁴		P_D	59	W
Linear Derating Factor			0.5	W / $^\circ\text{C}$
Single Pulse Avalanche Energy ³		E_{AS}	252	mJ
Single Pulse Avalanche Current		I_{AS}	48	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient ¹		$R_{\theta JA}$	62	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case ¹		$R_{\theta JC}$	2.1	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static							
Drain-Source Breakdown Voltage		BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250μA
Gate-Threshold Voltage		V _{GS(th)}	1.0	-	2.5	V	V _{DS} =V _{GS} , I _D =250μA
Forward Transconductance		g _{fs}	-	43	-	S	V _{DS} =5V, I _D =30A
Gate-Source Leakage Current		I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current	T _J =25℃	I _{DSS}	-	-	1	μA	V _{DS} =24V, V _{GS} =0
	T _J =55℃		-	-	5		V _{DS} =24V, V _{GS} =0
Static Drain-Source On-Resistance ²		R _{DS(ON)}	-	-	5.5	mΩ	V _{GS} =10V, I _D =30A
			-	-	8		V _{GS} =4.5V, I _D =15A
Total Gate Charge		Q _g	-	20	-	nC	I _D =15A V _{DS} =15V V _{GS} =4.5V
Gate-Source Charge		Q _{gs}	-	7.6	-		
Gate-Drain (“Miller”) Charge		Q _{gd}	-	7.2	-		
Turn-on Delay Time		T _{d(on)}	-	7.8	-	nS	V _{DD} =15V I _D =15A V _{GS} =10V R _G =3.3 Ω
Rise Time		T _r	-	15	-		
Turn-off Delay Time		T _{d(off)}	-	37.3	-		
Fall Time		T _f	-	10.6	-		
Input Capacitance		C _{iss}	-	2295	-	pF	V _{GS} =0 V _{DS} =15V f =1.0MHz
Output Capacitance		C _{oss}	-	267	-		
Reverse Transfer Capacitance		C _{rss}	-	210	-		
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy ⁵		EAS	63	-	-	mJ	V _{DD} =25V,L=0.1mH , I _{AS} =24A
Source-Drain Diode							
Diode Forward Voltage ²		V _{SD}	-	-	1	V	I _S =1A, V _{GS} =0
Continuous Source Current ^{1,6}		I _S	-	-	80	A	V _D =V _G =0, Force Current
Pulsed Source Current ^{2,6}		I _{SM}	-	-	160	A	
Reverse Recovery Time		T _{RR}	-	14	-	nS	I _F =30A, dI/dt=100A/μS
Reverse Recovery Charge		Q _{RR}	-	5	-	nC	T _J =25℃

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=48A$
- The power dissipation is limited by 150 $^\circ C$ junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

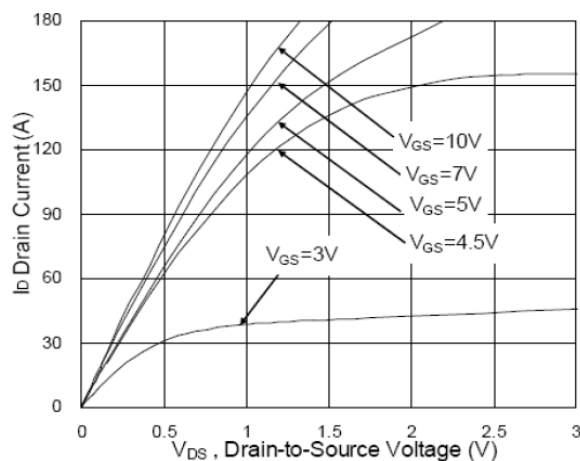


Fig.1 Typical Output Characteristics

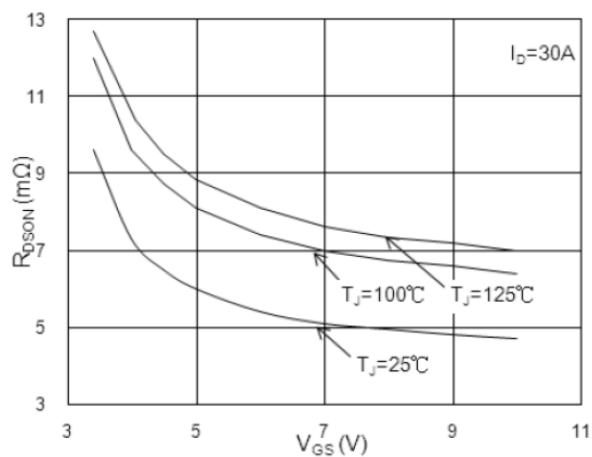


Fig.2 On-Resistance vs. G-S Voltage

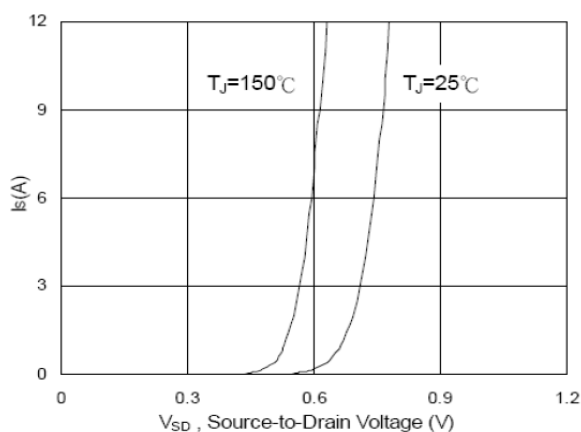


Fig.3 Forward Characteristics of Reverse

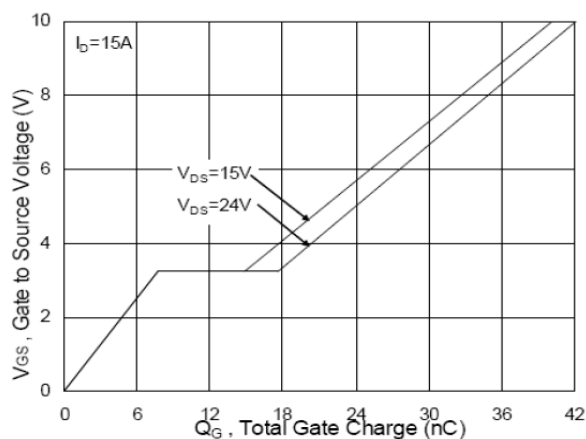


Fig.4 Gate-Charge Characteristics

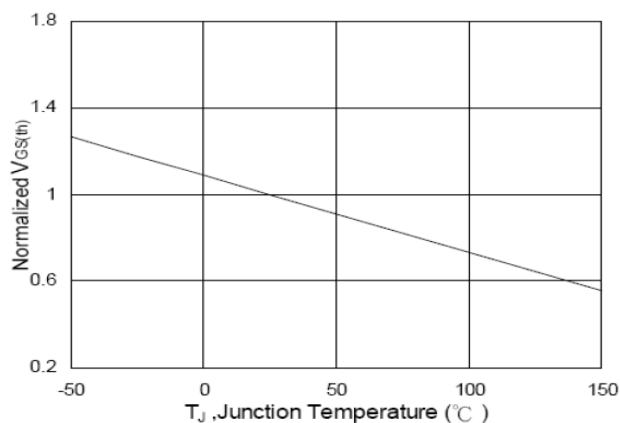


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

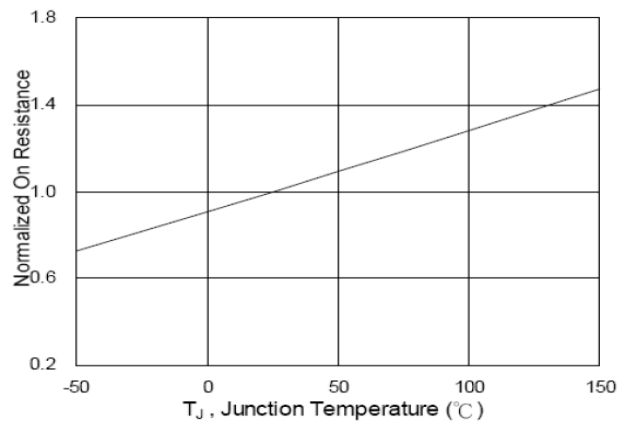


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

CHARACTERISTIC CURVES

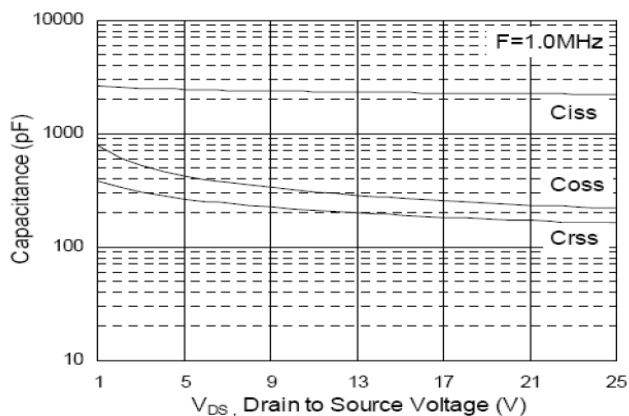


Fig.7 Capacitance

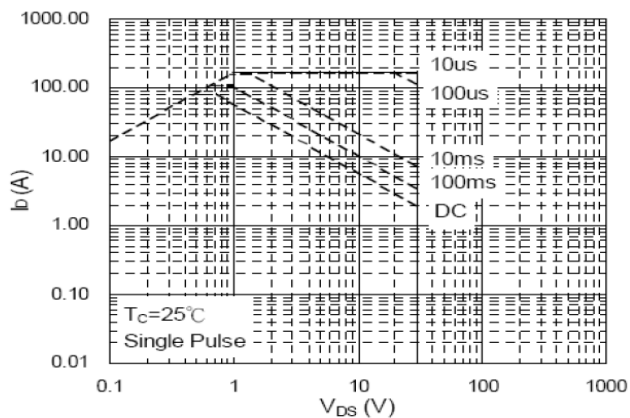


Fig.8 Safe Operating Area

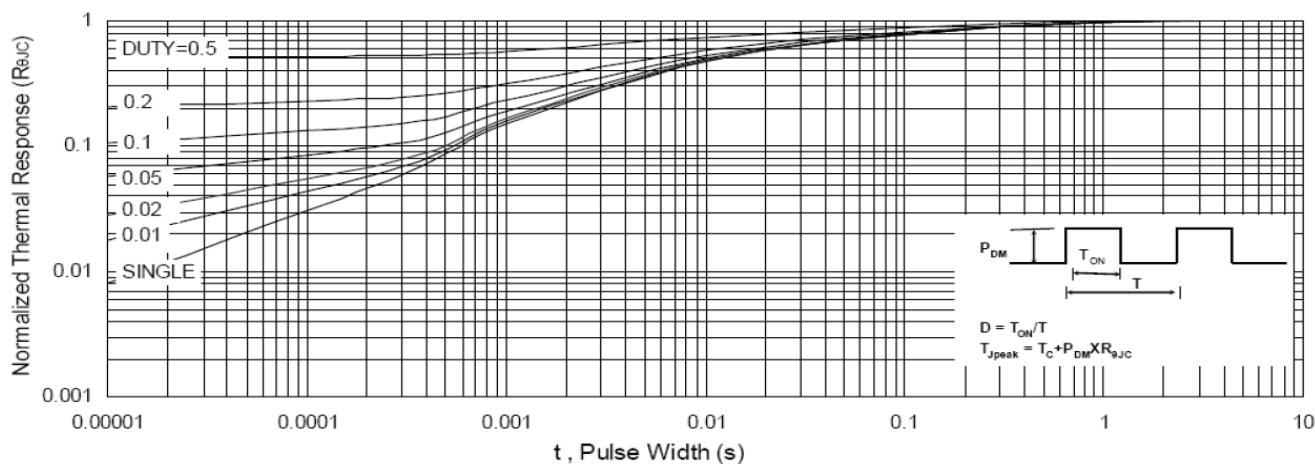


Fig.9 Normalized Maximum Transient Thermal Impedance

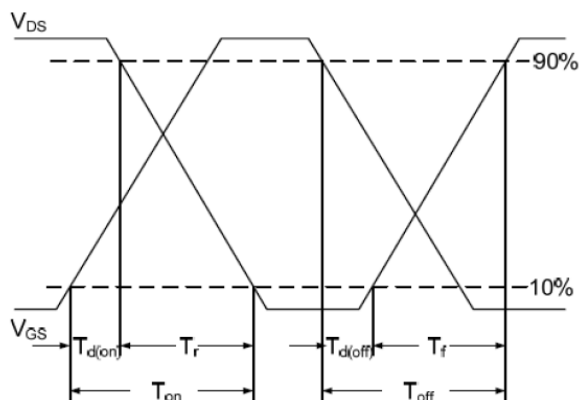


Fig.10 Switching Time Waveform

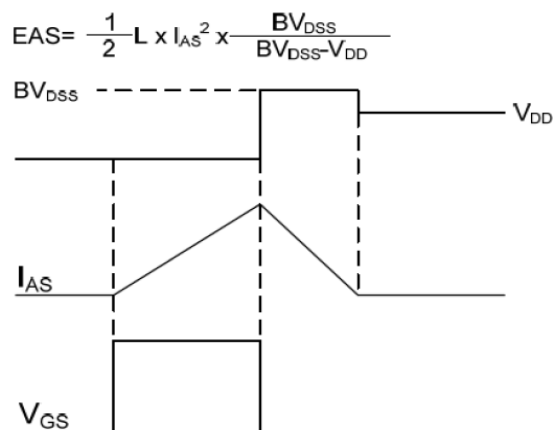


Fig.11 Unclamped Inductive Switching Waveform