

RoHS Compliant Product
A suffix of "-C" specifies halogen free

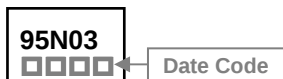
DESCRIPTION

The SSD95N03 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

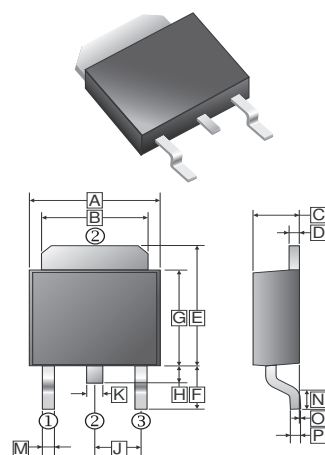
MARKING



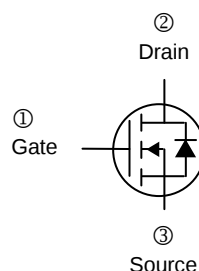
PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30 REF.	
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Rating	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	±20	V	
Continuous Drain Current ¹	V _{GS} =10V, T _C =25℃	I _D	96	A	
	V _{GS} =10V,T _C =100℃		88	A	
Pulsed Drain Current ²		I _{DM}	192	A	
Total Power Dissipation ⁴		T _C =25℃	P _D	62.5	W
Linear Derating Factor			0.42	W / ℃	
Single Pulse Avalanche Energy ³		E _{AS}	317	mJ	
Single Pulse Avalanche Current		I _{AS}	53.8	A	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~175	℃	
Thermal Resistance Rating					
Maximum Thermal Resistance Junction-Ambient ¹		R _{θJA}	62	℃ / W	
Maximum Thermal Resistance Junction-Case ¹		R _{θJC}	2.4	℃ / W	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static							
Drain-Source Breakdown Voltage		BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250μA
Breakdown Voltage Temperature Coefficient		△BV _{DSS} / △T _J	-	0.0213	-	V / ℃	Reference to 25℃, I _D =1mA
Gate-Threshold Voltage		V _{GS(th)}	1.0	-	2.5	V	V _{DS} =V _{GS} , I _D =250μA
Forward Transconductance		g _{fs}	-	26.5	-	S	V _{DS} =5V, I _D =30A
Gate-Source Leakage Current		I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current	T _J =25℃	I _{DSS}	-	-	1	μA	V _{DS} =24V, V _{GS} =0
	T _J =55℃		-	-	5		V _{DS} =24V, V _{GS} =0
Static Drain-Source On-Resistance ²		R _{DS(ON)}	-	3.4	4	mΩ	V _{GS} =10V, I _D =30A
			-	5.2	6		V _{GS} =4.5V, I _D =15A
Total Gate Charge		Q _g	-	31.6	-	nC	I _D =15A V _{DS} =15V V _{GS} =4.5V
Gate-Source Charge		Q _{gs}	-	8.6	-		
Gate-Drain (“Miller”) Change		Q _{gd}	-	11.7	-		
Turn-on Delay Time		T _{d(on)}	-	9	-	nS	V _{DD} =15 V I _D =15A V _{GS} =10V R _G =3.3 Ω
Rise Time		T _r	-	19	-		
Turn-off Delay Time		T _{d(off)}	-	58	-		
Fall Time		T _f	-	15.2	-		
Input Capacitance		C _{iss}	-	3075	4000	pF	V _{GS} =0 V _{DS} =15 V f =1.0MHz
Output Capacitance		C _{oss}	-	400	530		
Reverse Transfer Capacitance		C _{rss}	-	315	-		
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy ⁵		EAS	98	-	-	mJ	V _{DD} =25V,L=0.1mH , I _{AS} =30A
Source-Drain Diode							
Diode Forward Voltage ²		V _{SD}	-	-	1.2	V	I _S =30A, V _{GS} =0
Continuous Source Current ^{1,6}		I _S	-	-	96	A	V _D =V _G =0, Force Current
Pulsed Source Current ^{2,6}		I _{SM}	-	-	192	A	

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=53.8A$
- The power dissipation is limited by $175^\circ C$ junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

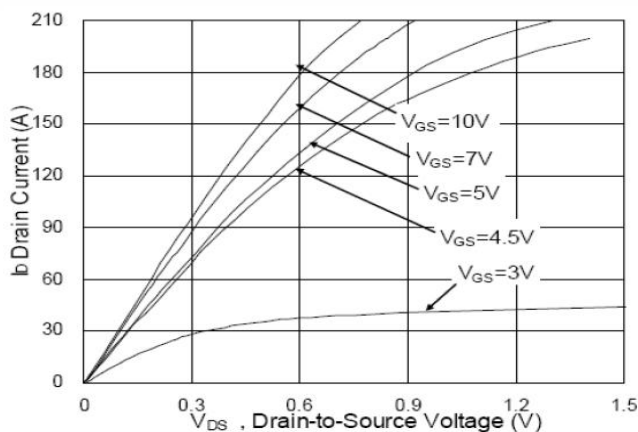


Fig.1 Typical Output Characteristics

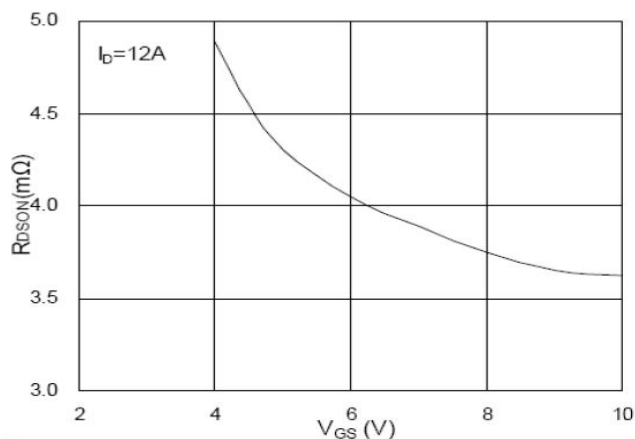


Fig.2 On-Resistance vs. G-S Voltage

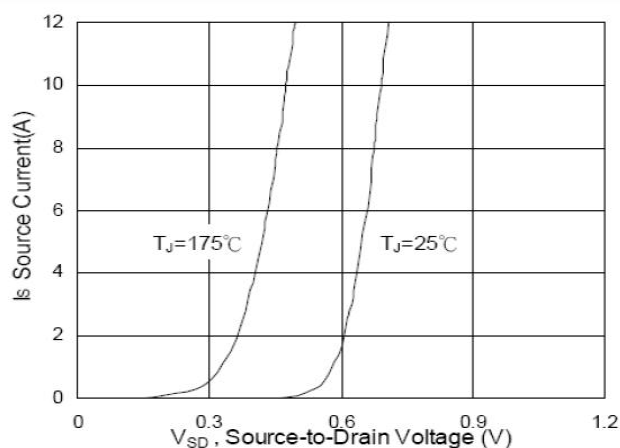


Fig.3 Forward Characteristics of Reverse

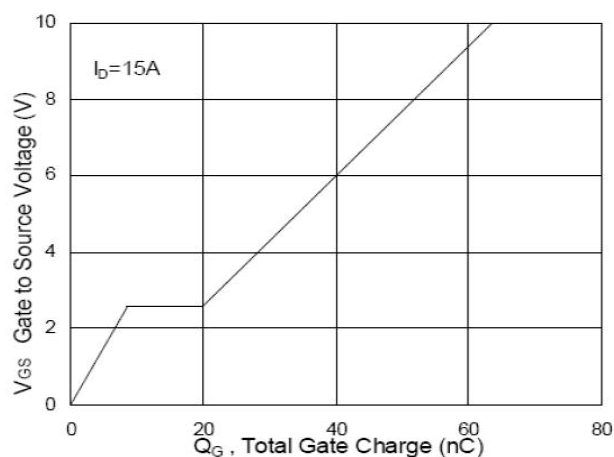


Fig.4 Gate-Charge Characteristics

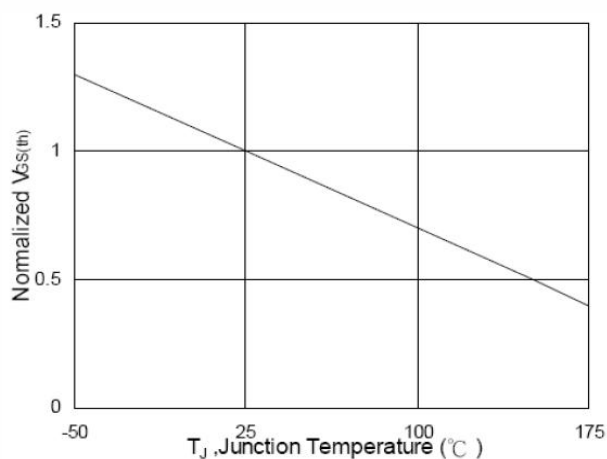


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

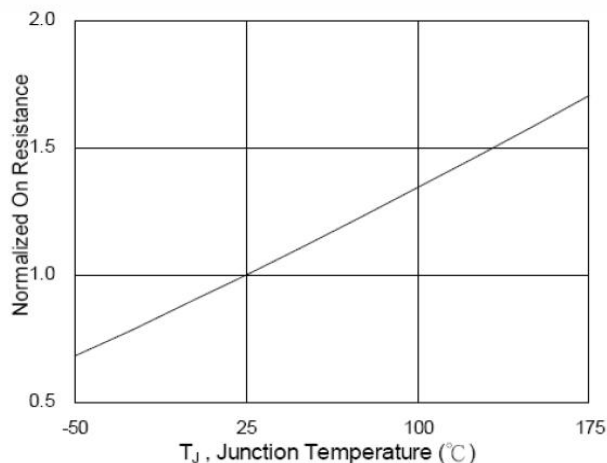


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

CHARACTERISTIC CURVES

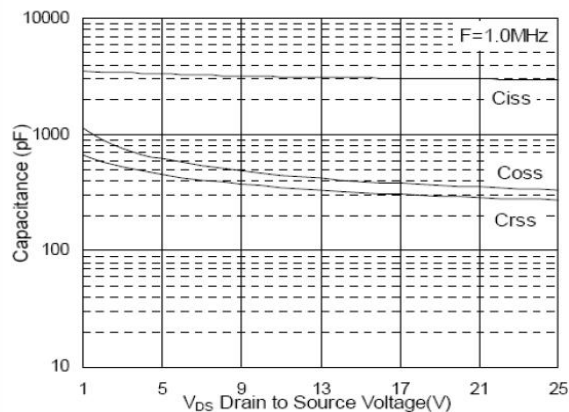


Fig.7 Capacitance

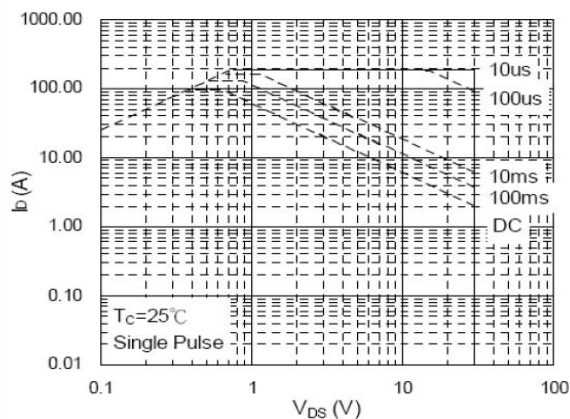


Fig.8 Safe Operating Area

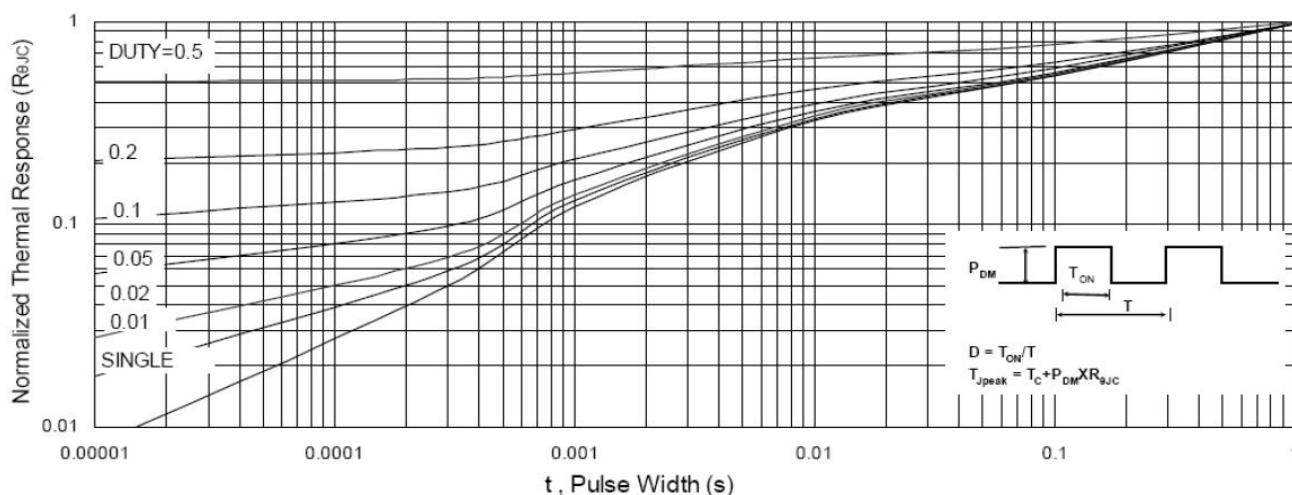


Fig.9 Normalized Maximum Transient Thermal Impedance

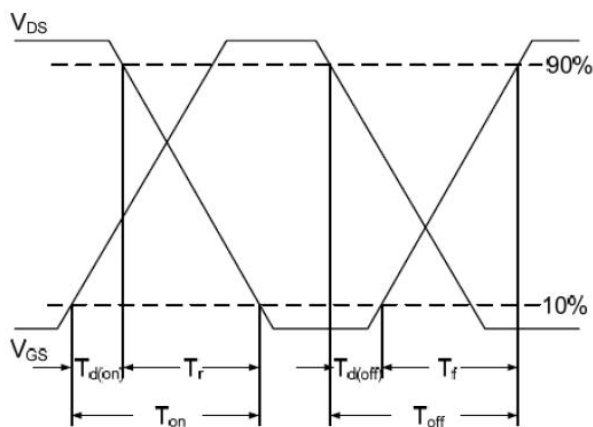


Fig.10 Switching Time Waveform

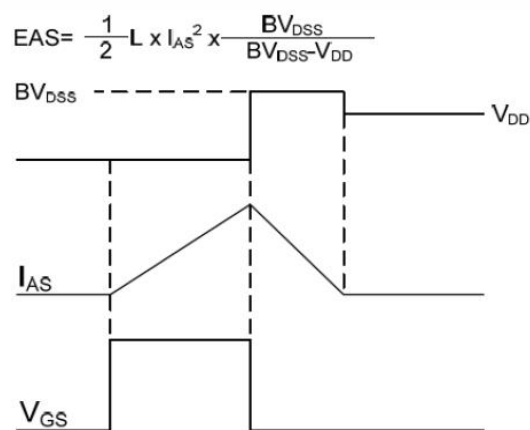


Fig.11 Unclamped Inductive Switching Wave