

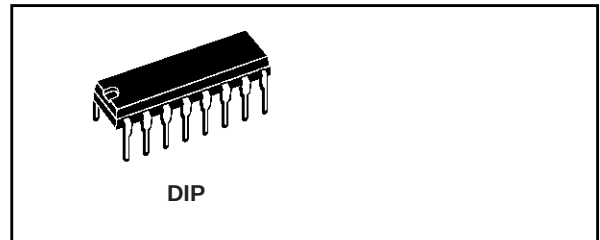


TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

- LOW "ON" RESISTANCE : 125Ω (Typ.) OVER 15V p.p SIGNAL-INPUT RANGE FOR $V_{DD} - V_{EE} = 15V$
- HIGH "OFF" RESISTANCE : CHANNEL LEAKAGE $\pm 100pA$ (Typ.) at $V_{DD} - V_{EE} = 18V$
- BINARY ADDRESS DECODING ON CHIP
- HIGH DEGREE OF LINEARITY : $< 0.5\%$ DISTORTION TYP. at $f_{IS} = 1KHz$, $V_{IS} = 5 V_{pp}$, $V_{DD} - V_{SS} \geq 10V$, $R_L = 10K\Omega$
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS : $0.2 \mu W$ (Typ.) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V$
- MATCHED SWITCH CHARACTERISTICS : $R_{ON} = 5\Omega$ (Typ.) FOR $V_{DD} - V_{EE} = 15V$
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS : DIGITAL 3 to 20, ANALOG TO 20V p.p.
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT $I_I = 100nA$ (MAX) AT $V_{DD} = 18V$ $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

The CC4053 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor



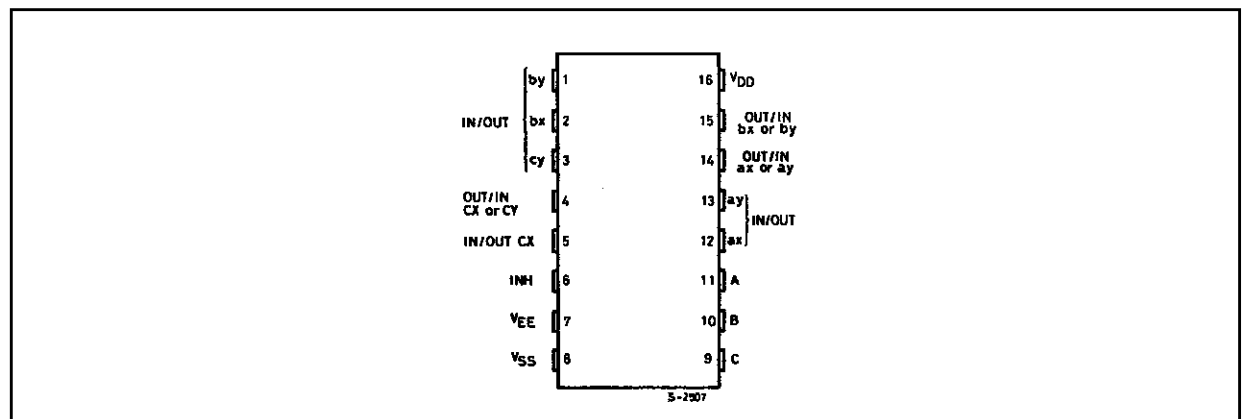
ORDER CODES

PACKAGE	TUBE	T & R
DIP	CC4053	

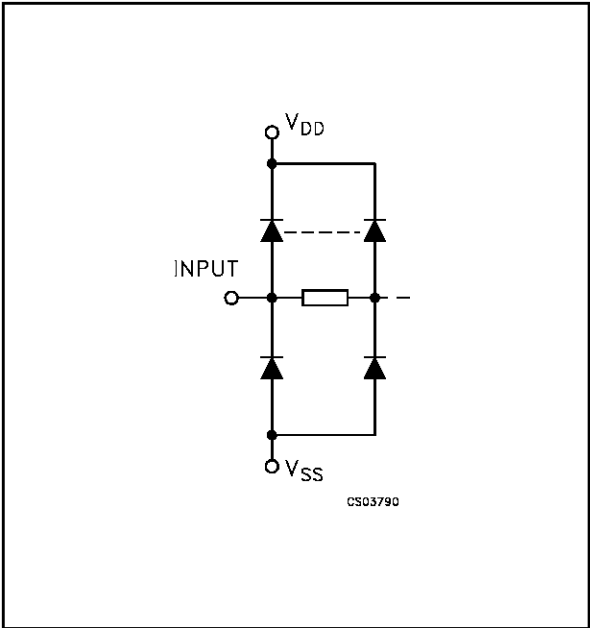
technology available in DIP and SOP packages. The CC4053 analog multiplexer/demultiplexer is a digitally controlled analog switch having low ON impedance and very low OFF leakage current. This multiplexer circuit dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage range, independent of the logic state of the control signals.

When a logic "1" is present at the inhibit input terminal all channel are off. This device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single pole double-throw configuration.

PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

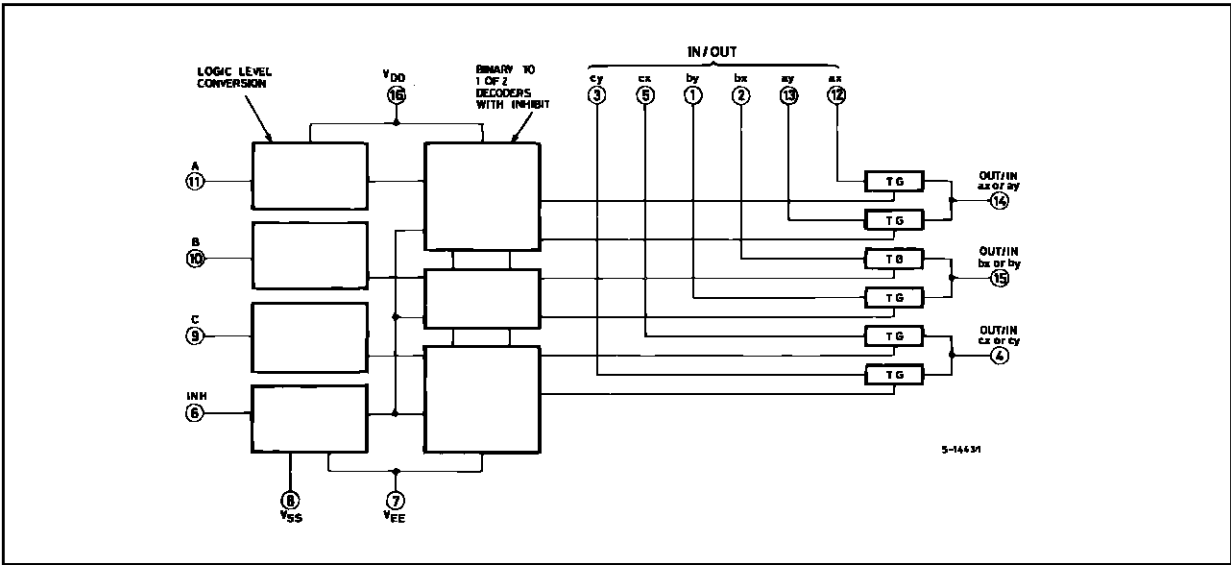
PIN No	SYMBOL	NAME AND FUNCTION
11, 10, 9	A, B, C	Binary Control Inputs
6	INH	Inhibit Inputs
12, 13, 2, 1, 5, 3	IN/OUT	ax,ay,bx,by,cx,cy Input/ Output
14	OUT/IN	ax or ay
15	OUT/IN	bx or by
4	OUT/IN	cx or cy
7	V _{EE}	Supply Voltage
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

TRUTH TABLE

INHIBIT	C or B or A	
0	0	ax or bx or cx
0	1	ay or by or cy
1	X	NONE

X : Don't Care

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 1.8	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value								Unit
		V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
I _L	Quiescent Device Current (all switches ON or all switches OFF)				5		0.04	5		150		150	μA	
					10		0.04	10		300		300		
					15		0.04	20		600		600		
					18		0.08	100		3000		3000		
SWITCH														
R _{ON}	Resistance	0 ≤ V _I ≤ V _{DD}	0	0	5		470	1050		1200		1200	Ω	
					10		180	400		520		520		
					15		125	280		360		360		
Δ _{ON}	Resistance Δ _{RON} (between any 2 of 4 switches)	0 ≤ V _I ≤ V _{DD}	0	0	5		10						Ω	
					10		10							
					15		5							
OFF*	Channel Leakage Current (All Channel OFF) (COMMON O/I)		0	0	18		±0.1	100		1000		1000	nA	
OFF*	Channel Leakage Current (Any Channel OFF)		0	0	18		±0.1	100		1000		1000	nA	
C _I	Input Capacitance		-5	-5	5		5						pF	
C _O	Output Capacitance						9							
C _{IO}	Feed through						0.2							
CONTROL (Address or Inhibit)														
V _{IL}	Input Low Voltage	= VDD thru 1KΩ	V _{EE} = V _{SS} R _L = 1KΩ to V _{SS} I _{IS} < 2μA (on all OFF channels)	5			1.5		1.5		1.5	V		
				10			3		3		3			
				15			4		4		4			
V _{IH}	Input High Voltage			5	3.5			3.5		3.5			V	
				10	7			7		7				
				15	11			11		11				
I _{IH} , I _{IL}	Input Leakage Current	V _I = 0/18V			18		±10 ⁻³	±0.1		±1		±1	μA	
C _I	Input Capacitance						5	7.5					pF	

* Determined by minimum feasible leakage measurement for automating testing.

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, all input square wave rise and fall time = 20 ns)

Parameter	Test Condition							Value			Unit
	V _{EE} (V)	R _L (KΩ)	f _I (KHz)	V _I (V)	V _{SS} (V)	V _{DD} (V)		Min.	Typ.	Max.	
Propagation Delay Time (signal input to output)		200				5			30	60	ns
						10			15	30	
						15			11	20	
Frequency Response Channel "ON" (sine wave input) at 20 log V _O /V _I = - 3dB	= V _{SS}	1		5(*)		10	V _O at Common OUT/IN		25		MHz
							V _O at any channel		60		
Feed through (all channels OFF) at 20 log V _O /V _I = - 40dB	= V _{SS}	1		5(*)		10	V _O at Common OUT/IN		10		MHz
							V _O at any channel		8		
Frequency Signal Crosstalk at 20 log V _O /V _I = -40dB	= V _{SS}	1		5(*)		10	Between any 2 Sections (IN pin 2, OUT pin 14)		2.5		MHz
							Between any 2 Sections (IN pin 15, OUT pin 14)		6		
Sine Wave Distortion f _{IS} = 1KHz Sine Wave	= V _{SS}	10	1	2(*)		5			0.3		%
				3(*)		10			0.2		
				5(*)		15			0.12		
CONTROL (Address or Inhibit)											
Propagation Delay: Address to Signal OUT (Channels ON or OFF)	0				0	5			360	720	ns
	0				0	10			160	320	
	0				0	15			120	240	
	-5				0	5			225	450	
Propagation Delay: Inhibit to Signal OUT (Channel turning ON)	0	1			0	5			360	720	ns
	0				0	10			160	320	
	0				0	15			120	240	
	-10				0	5			200	400	
Propagation Delay: Inhibit to Signal OUT (Channel turning OFF)	0	10				5			200	450	ns
	0					10			90	210	
	0					15			70	160	
	-10					5			130	300	
Address or Inhibit to Signal Crosstalk	0	10 ⁽¹⁾			0	10	V _C = V _{DD} -V _{SS} (square wave)		65		mV peak

(1) Both ends of channel.

* Peak to Peak voltage symmetrical about $(V_{DD} - V_{EE}) / 2$