P-Channel Enhancement Mode Field Effect Transistor

- **Features**

V_{DS} (V) = -30 V

I_D = -3.5 A

$R_{DS(ON)}$ = 75mΩ @V_{GS} = -10V

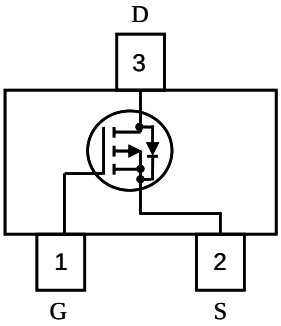
$R_{DS(ON)}$ = 90mΩ @V_{GS} = -4.5V

High density cell design for low $R_{DS(ON)}$.

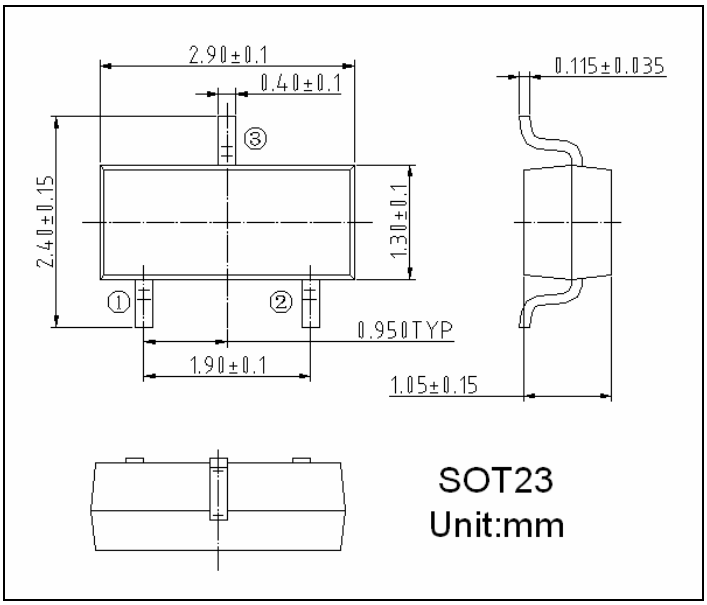
- **General Description**

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

- **Pin Configuration**



- **Package Information**



- **Absolute Maximum Ratings** @T_A = 25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	-3.5	A
	Pulsed(1)		-16	
Power Dissipation		P_D	1	W
Operating and Storage Temperature Range		T_J,T_{STG}	-55 to 150	℃

- **Electrical Characteristics** @T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -250 μA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	--	--	-1	μA
Gate - Body Leakage, Forward	I_{GSSF}	V_{GS} = +20 V, V_{DS} = 0 V	--	--	100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
ON CHARACTERISTICS (2)						
Gate Threshold Voltage	$V_{GS\ (th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-1	-1.4	-2.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -3 A	--	90	110	mΩ
		V_{GS} = -10 V, I_D = -4.1 A	--	75	90	
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -2.8 A	4	6	--	S
DYNAMIC CHARACTERISTICS (3)						
Input Capacitance	C_{iss}	V_{DS} = -6 V, V_{GS} = 0 V, f = 1.0 MHz	--	680	--	pF
Output Capacitance	C_{oss}		--	72	--	pF
Reverse Transfer Capacitance	C_{rss}		--	58	--	pF
SWITCHING CHARACTERISTICS (3)						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6 V, R_L = 6Ω, I_D = -1.0 A, V_{GEN} = -4.5 V, R_G = 6Ω	--	--	20	ns
Turn-On Rise Time	t_r		---	--	10	
Turn-Off Delay Time	$t_{d(off)}$	V_{DD}= -6 V, R_L = 6Ω, I_D = -1.0 A, V_{GEN} = -4.5 V, R_G = 6Ω	--	--	65	ns
Turn-Off Fall Time	t_f		--	--	45	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Current(4)	I_S	--	--	--	-1.35	A
Drain-Source Diode Forward Voltage(2)	V_{SD}	V_{GS} = 0 V, I_S = -0.75 A	-0.6	-0.8	-1.3	V

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test: PW≤300μs, duty cycle≤2%.
3. Guaranteed by design, not subject to production testing.
4. Surface Mounted on FR4 Board, t < 5 sec.

- **Typical Performance Characteristics**

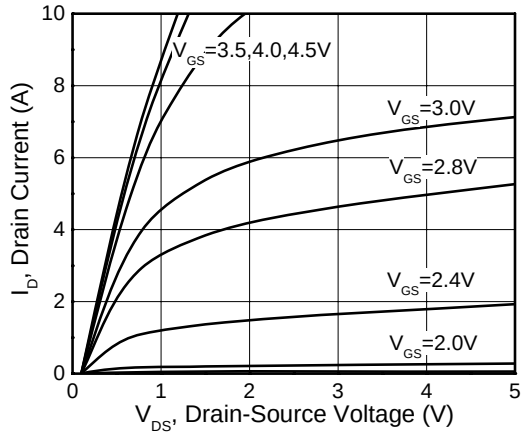


Figure 1. Output Characteristics

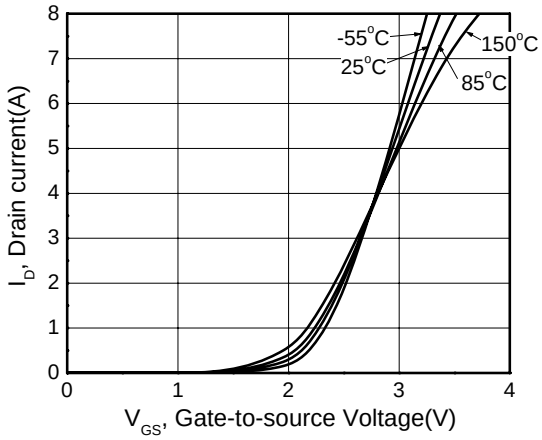


Figure 2. Transfer Characteristics

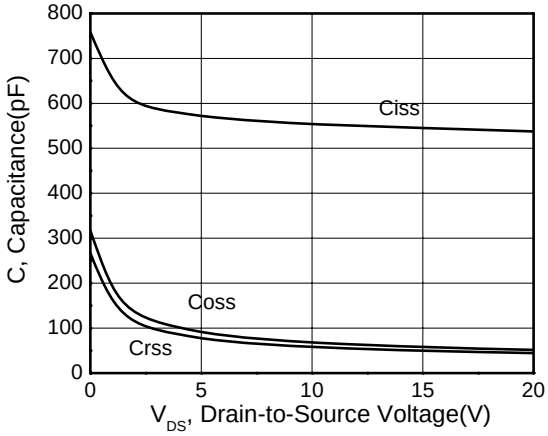


Figure 3. Capacitance

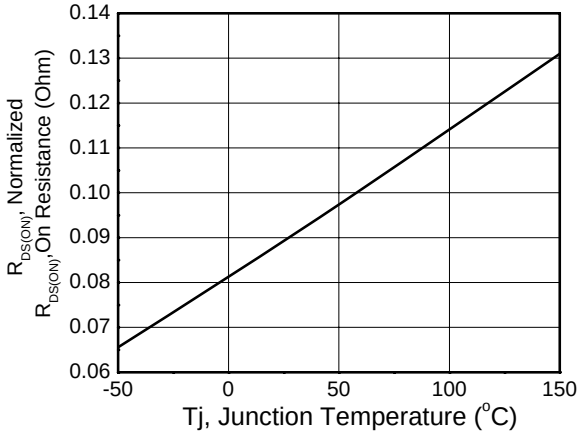


Figure 4. On Resistance Vs. Temperature

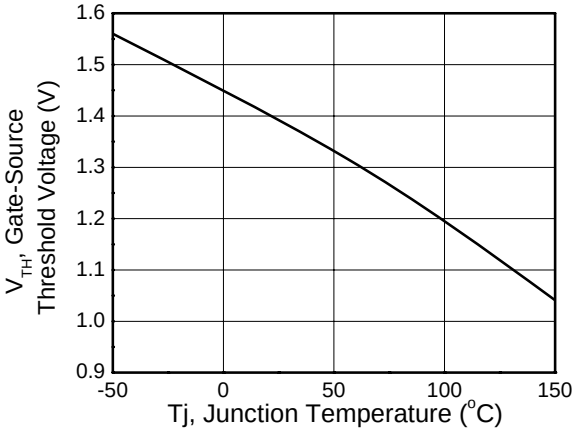


Figure 5. Gate Thershold Vs. Temperature

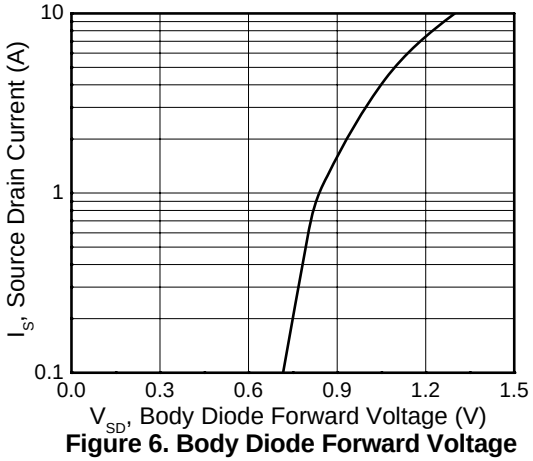


Figure 6. Body Diode Forward Voltage Vs. Source Current

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