

ADD-A-PAK Generation VII Power Modules Thyristor/Diode and Thyristor/Thyristor, 45 A/60 A




ADD-A-PAK

PRODUCT SUMMARY	
$I_{T(AV)}$ or $I_{F(AV)}$	45 A/60 A
Type	Modules - Thyristor, Standard

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- High voltage
- Industrial standard package
- Low thermal resistance
- UL approved file E78996 
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION

These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS, and battery charger.

MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS	VSK.41	VSK.56	UNITS
$I_{T(AV)}$ or $I_{F(AV)}$	85 °C	45	60	A
$I_{O(RMS)}$	As AC switch	100	135	
I_{TSM} , I_{FSM}	50 Hz 60 Hz	850 890	1200 1256	
I^2t	50 Hz	3.61	7.20	kA ² s
	60 Hz	3.30	6.57	
$I^2\sqrt{t}$		36.1	72	kA ² √s
V_{RRM}	Range	400 to 1600		V
T_{Stg}		-40 to 125		°C
T_J		-40 to 125		



ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS					
TYPE NUMBER	VOLTAGE CODE	V _{RRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	V _{DRM} , MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V	I _{RRM} , I _{DRM} AT 125 °C mA
VSK.41 VSK.56	04	400	500	400	15
	06	600	700	600	
	08	800	900	800	
	10	1000	1100	1000	
	12	1200	1300	1200	
	14	1400	1500	1400	
	16	1600	1700	1600	

ON-STATE CONDUCTION							
PARAMETER	SYMBOL	TEST CONDITIONS			VSK.41	VSK.56	UNITS
Maximum average on-state current (thyristors)	I _{T(AV)}	180° conduction, half sine wave, T _C = 85 °C			45	60	
Maximum average forward current (diodes)	I _{F(AV)}						
Maximum continuous RMS on-state current, as AC switch	I _{O(RMS)}				100	135	A
Maximum peak, one-cycle non-repetitive on-state or forward current	I _{TSM} or I _{FSM}	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial T _J = T _J maximum	850	1200	
		t = 8.3 ms			890	1256	
		t = 10 ms	100 % V _{RRM} reappplied		715	1000	
		t = 8.3 ms			750	1056	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reappplied	Initial T _J = T _J maximum	3.61	7.20	kA ² s
		t = 8.3 ms			3.30	6.57	
		t = 10 ms	100 % V _{RRM} reappplied		2.56	5.10	
		t = 8.3 ms			2.33	4.56	
Maximum I ² √t for fusing	I ² √t (1)	t = 0.1 ms to 10 ms, no voltage reappplied T _J = T _J maximum			36.1	72	kA ² √s
Maximum value or threshold voltage	V _{T(TO)} (2)	Low level (3)	T _J = T _J maximum		1.08	0.91	V
		High level (4)			1.12	1.02	
Maximum value of on-state slope resistance	r _t (2)	Low level (3)	T _J = T _J maximum		4.7	4.27	mΩ
		High level (4)			4.5	3.77	
Maximum peak on-state or forward voltage	V _{TM}	I _{TM} = π × I _{T(AV)}	T _J = 25 °C		1.81	1.7	V
	V _{FM}	I _{FM} = π × I _{F(AV)}					
Maximum non-repetitive rate of rise of turned on current	di/dt	T _J = 25 °C, from 0.67 V _{DRM} , I _{TM} = π × I _{T(AV)} , I _g = 500 mA, t _r < 0.5 μs, t _p > 6 μs			150		A/μs
Maximum holding current	I _H	T _J = 25 °C, anode supply = 6 V, resistive load, gate open circuit			200		mA
Maximum latching current	I _L	T _J = 25 °C, anode supply = 6 V, resistive load			400	400	

Notes

- (1) I²t for time t_x = I²√t × √t_x
- (2) Average power = V_{T(TO)} × I_{T(AV)} + r_t × (I_{T(RMS)})²
- (3) 16.7 % × π × I_{AV} < I < π × I_{AV}
- (4) I > π × I_{AV}



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VSK.41	VSK.56	UNITS
Maximum peak gate power	P_{GM}			10		W
Maximum average gate power	$P_{G(AV)}$			2.5		
Maximum peak gate current	I_{GM}			2.5		A
Maximum peak negative gate voltage	$-V_{GM}$			10		V
Maximum gate voltage required to trigger	V_{GT}	$T_J = -40\text{ }^\circ\text{C}$	Anode supply = 6 V resistive load	4.0		
		$T_J = 25\text{ }^\circ\text{C}$		2.5		
		$T_J = 125\text{ }^\circ\text{C}$		1.7		
Maximum gate current required to trigger	I_{GT}	$T_J = -40\text{ }^\circ\text{C}$	Anode supply = 6 V resistive load	270		mA
		$T_J = 25\text{ }^\circ\text{C}$		150		
		$T_J = 125\text{ }^\circ\text{C}$		80		
Maximum gate voltage that will not trigger	V_{GD}	$T_J = 125\text{ }^\circ\text{C}$, rated V_{DRM} applied		0.25		V
Maximum gate current that will not trigger	I_{GD}	$T_J = 125\text{ }^\circ\text{C}$, rated V_{DRM} applied		6		mA

BLOCKING						
PARAMETER	SYMBOL	TEST CONDITIONS		VSK.41	VSK.56	UNITS
Maximum peak reverse and off-state leakage current at V_{RRM} , V_{DRM}	I_{RRM} , I_{DRM}	$T_J = 125\text{ }^\circ\text{C}$, gate open circuit		15		mA
Maximum RMS insulation voltage	V_{INS}	50 Hz		3000 (1 min) 3600 (1 s)		V
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = 125\text{ }^\circ\text{C}$, linear to 0.67 V_{DRM}		1000		V/ μs

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		VSK.41	VSK.56	UNITS
Junction operating and storage temperature range	T_J , T_{Stg}			-40 to 125		$^\circ\text{C}$
Maximum internal thermal resistance, junction to case per leg	R_{thJC}	DC operation		0.44	0.35	$^\circ\text{C/W}$
Typical thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface flat, smooth and greased		0.1		
Mounting torque $\pm 10\%$	to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.		4		Nm
	busbar			3		
Approximate weight					75	g
					2.7	oz.
Case style	JEDEC®		AAP GEN VII (TO-240AA)			

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.41..	0.110	0.131	0.17	0.23	0.342	0.085	0.138	0.177	0.235	0.345	$^\circ\text{C/W}$
VSK.56..	0.088	0.104	0.134	0.184	0.273	0.07	0.111	0.143	0.189	0.275	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

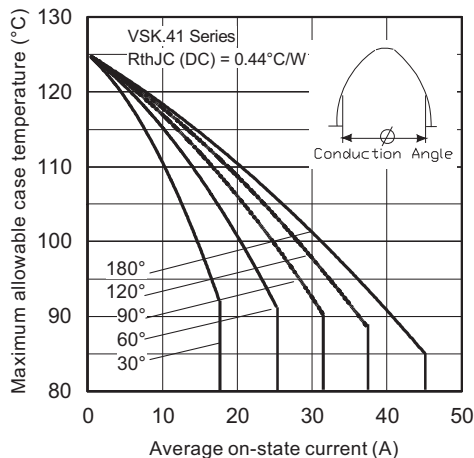


Fig. 1 - Current Ratings Characteristics

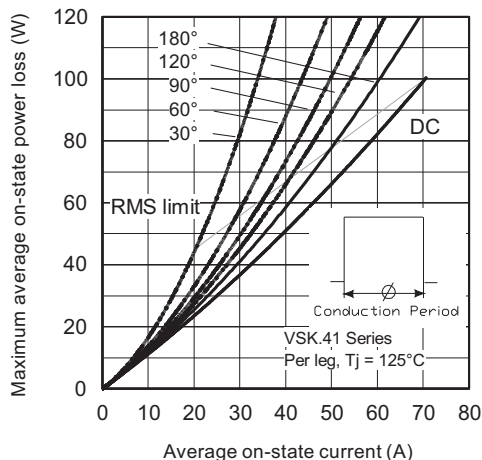


Fig. 4 - On-State Power Loss Characteristics

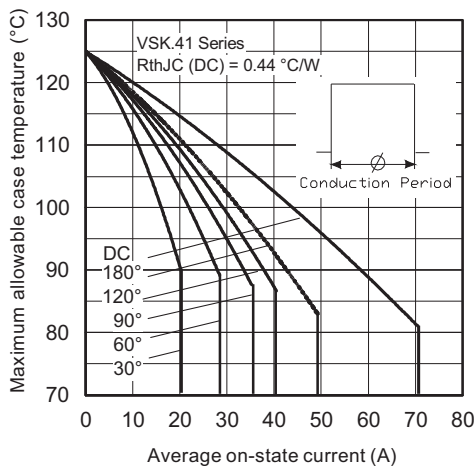


Fig. 2 - Current Ratings Characteristics

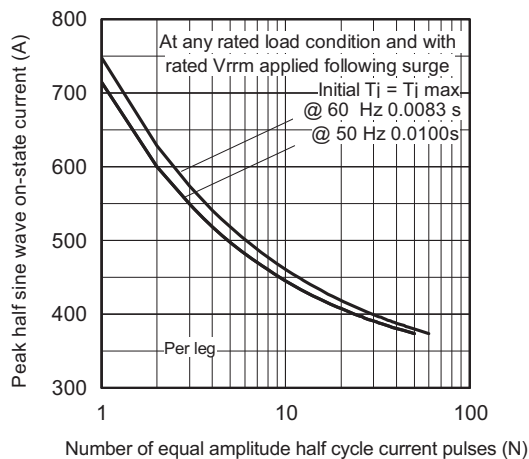


Fig. 5 - Maximum Non-Repetitive Surge Current

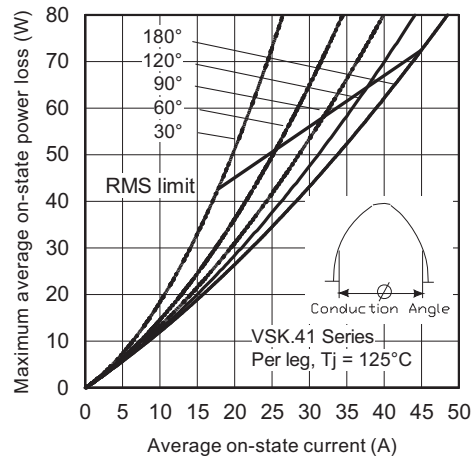


Fig. 3 - On-State Power Loss Characteristics

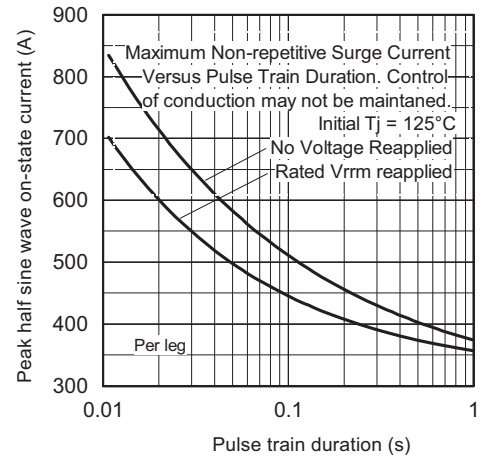


Fig. 6 - Maximum Non-Repetitive Surge Current

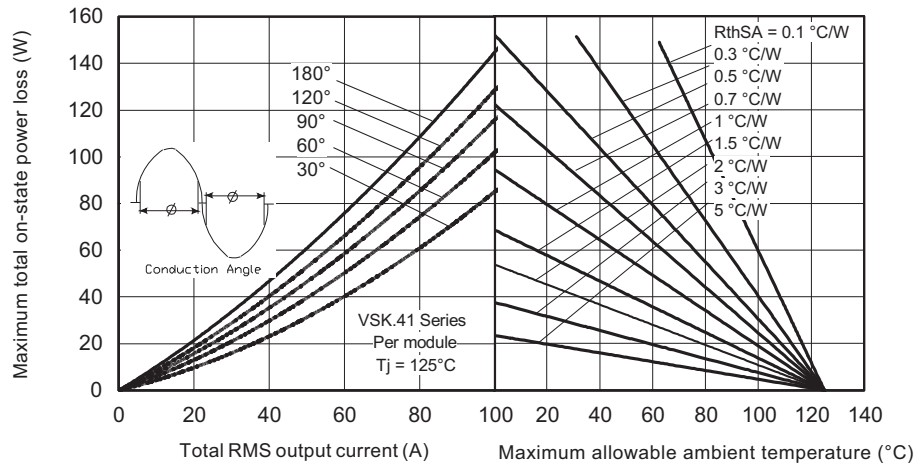


Fig. 7 - On-State Power Loss Characteristics

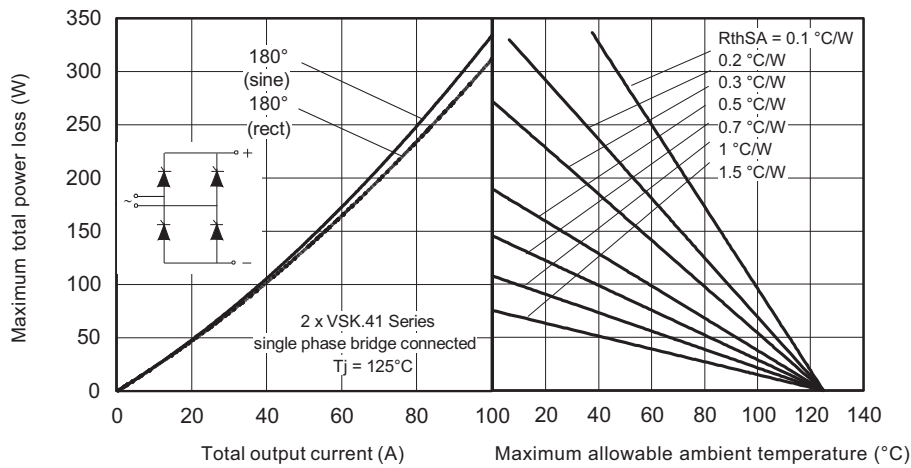


Fig. 8 - On-State Power Loss Characteristics

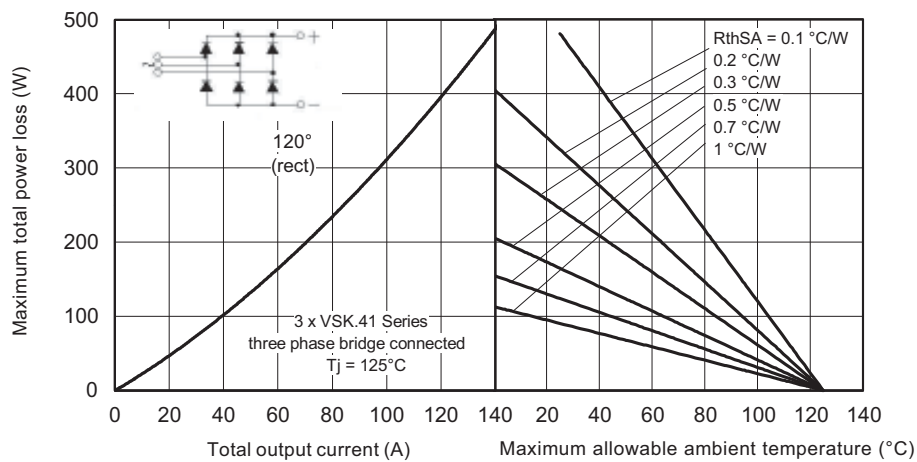


Fig. 9 - On-State Power Loss Characteristics

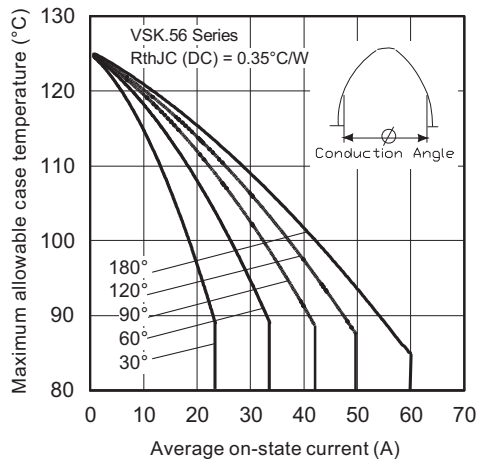


Fig. 10 - Current Ratings Characteristics

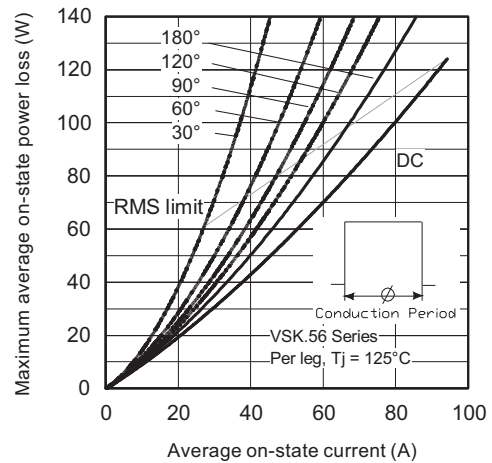


Fig. 13 - On-State Power Loss Characteristics

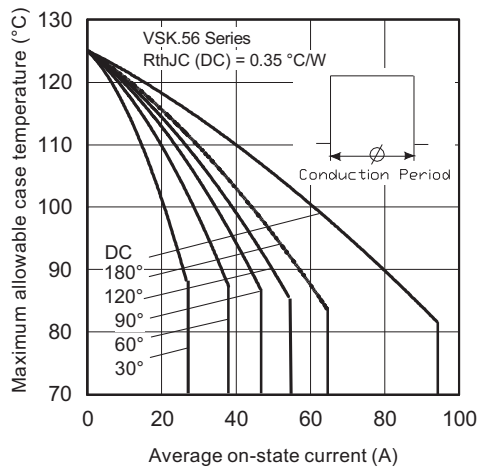


Fig. 11 - Current Ratings Characteristics

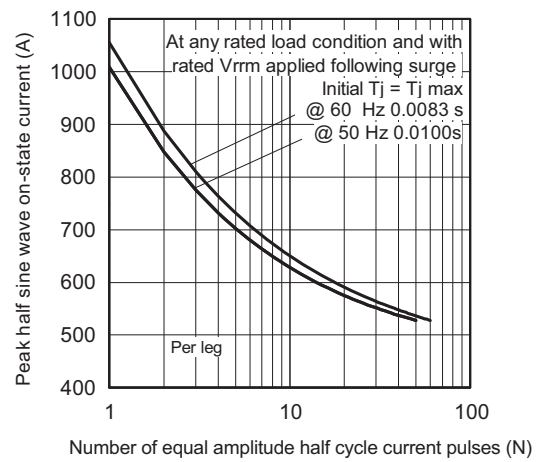


Fig. 14 - Maximum Non-Repulsive Surge Current

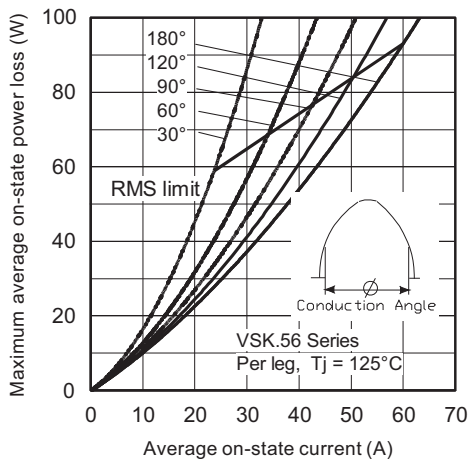


Fig. 12 - On-State Power Loss Characteristics

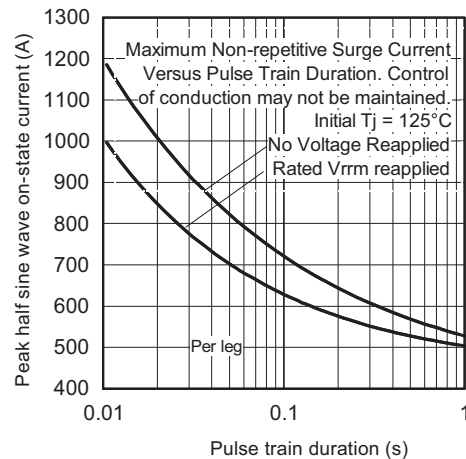


Fig. 15 - Maximum Non-Repulsive Surge Current

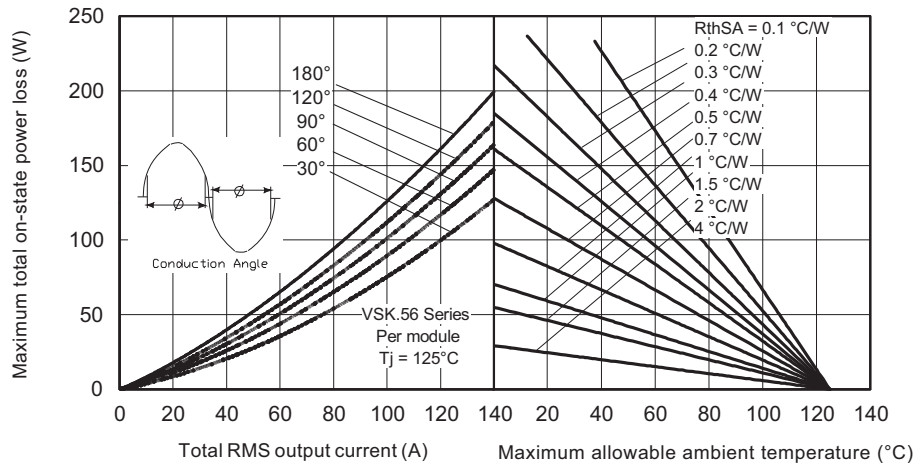


Fig. 16 - On-State Power Loss Characteristics

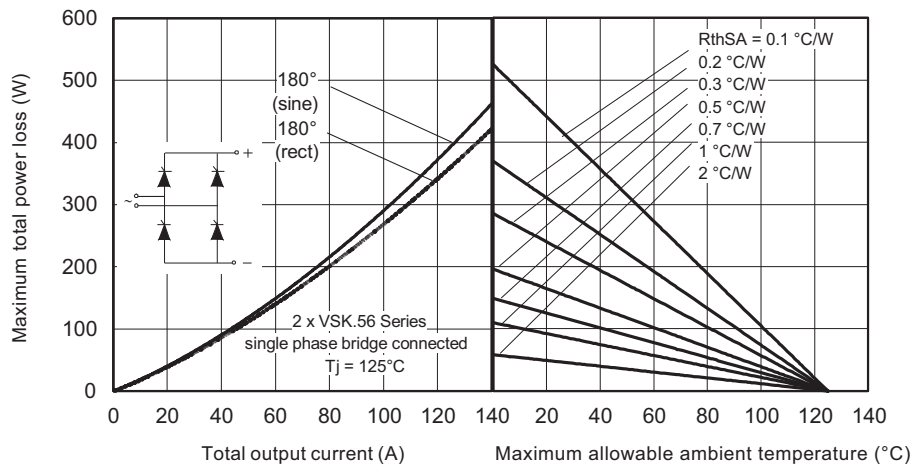


Fig. 17 - On-State Power Loss Characteristics

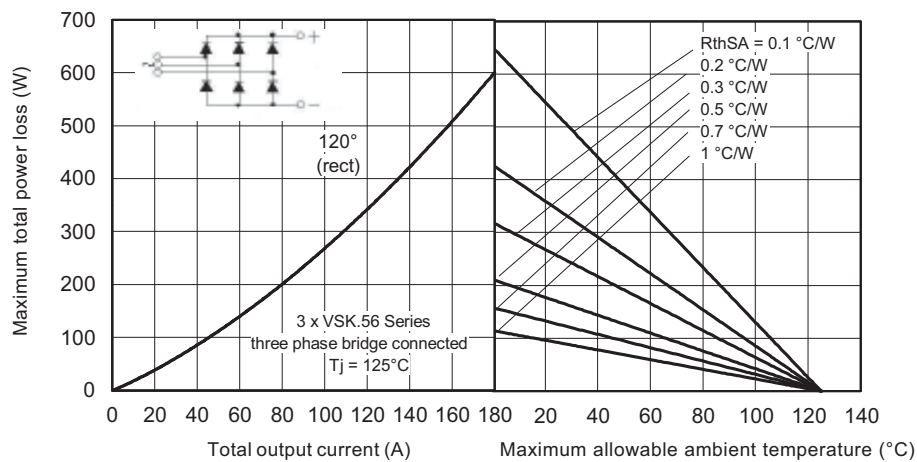


Fig. 18 - On-State Power Loss Characteristics

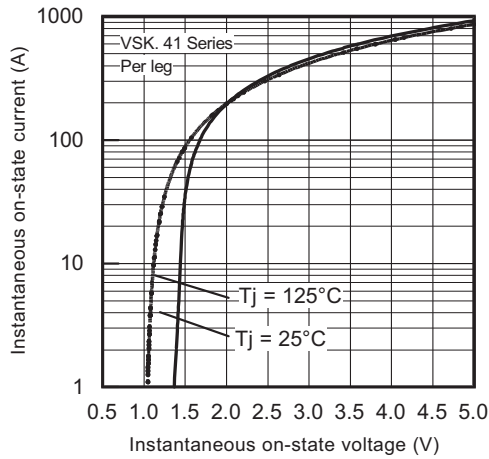


Fig. 19 - On-State Voltage Drop Characteristics

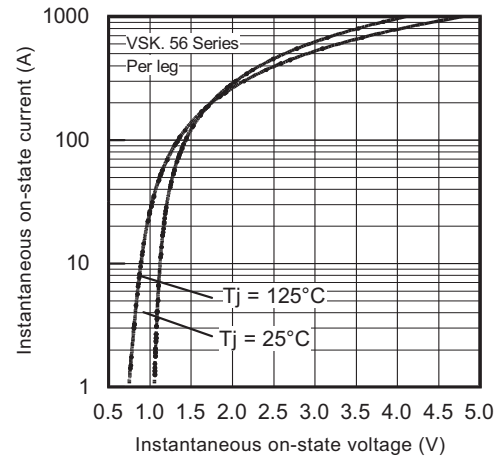


Fig. 20 - On-State Voltage Drop Characteristics

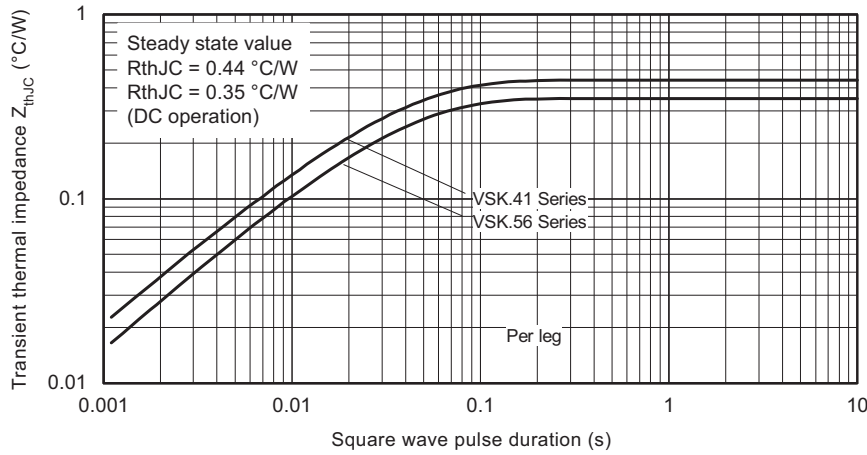


Fig. 21 - Thermal Impedance Z_{thJC} Characteristics

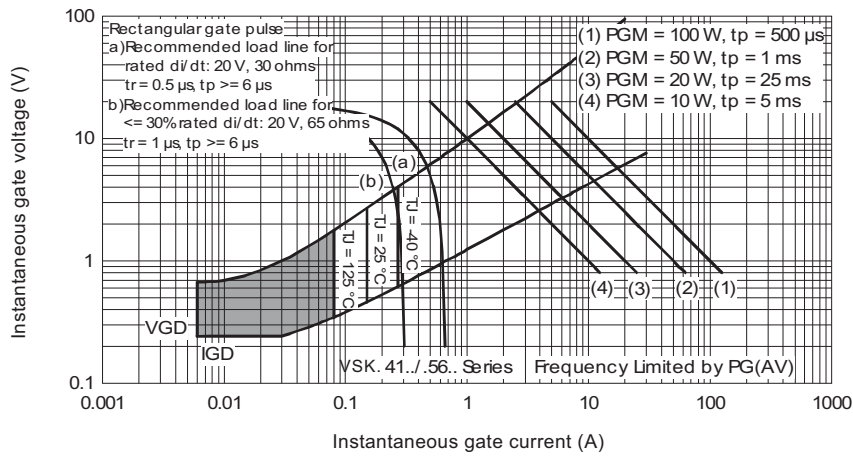


Fig. 22 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	VSK	T	56	/	16
	①	②	③		④

1	-	Module type	
2	-	Circuit configuration (see end of datasheet)	
3	-	Current code	41 = 45 A 56 = 60 A
4	-	Voltage code (see Voltage Ratings table)	

Note

- To order the optional hardware go to www.vishay.com/doc?95172

CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	T	
SCR/diode doubler circuit, positive control	H	
SCR/diode doubler circuit, negative control	L	
SCR/diode common anodes	N	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95368

ADD-A-PAK Generation VII - Thyristor

DIMENSIONS in millimeters (inches)





Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.